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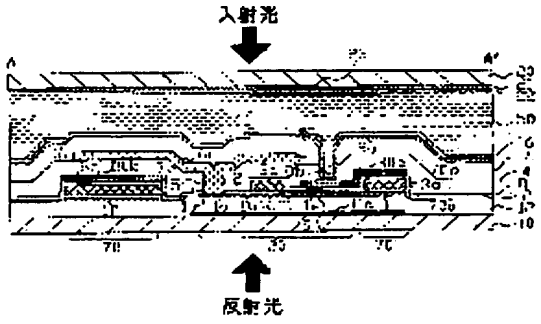
(54) ELECTRO-OPTIC DEVICE, METHOD OF MANUFACTURING THE SAME AND ELECTRONIC APPLIANCE

(57)Abstract:

PROBLEM TO BE SOLVED: To increase the pixel opening rate while connecting a pixel electrode to a semiconductor layer and to make high-quality image display possible in a rather simple structure in an electro-optic device using a TFT active matrix driving system.

SOLUTION: The pixel electrode and the TFT are connected by way of a first barrier layer 80a through a contact hole 8a and a contact hole 8b. A second barrier layer 80b is formed wider than a data line 6a, and one end of the layer 80b is overlapped on the pixel electrode 9a to determine the pixel opening region.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The thin film transistor and pixel electrode which have been arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, The 1st conductive layer of the protection-from-light nature which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, and was connected to said semi-conductor layer and electric target, and was connected to said pixel electrode and electric target, The electro-optic device characterized by having the 2nd conductive layer which consisted of the same film as said 1st conductive layer, saw superficially, and has lapped with said data line selectively at least.
[Claim 2] Said 2nd conductive layer is an electro-optic device according to claim 1 characterized by having seen superficially and having lapped with said pixel electrode selectively at least.
[Claim 3] Said 1st conductive layer is an electro-optic device according to claim 1 or 2 characterized by having connected electrically through said semi-conductor layer and 1st contact hole, and connecting electrically through said pixel electrode and 2nd contact hole.
[Claim 4] Said data line is an electro-optic device given in any 1 term of claims 1-3 characterized by connecting electrically through said semi-conductor layer and 3rd contact hole.
[Claim 5] Said data line is an electro-optic device given in any 1 term of claims 1-4 characterized by seeing superficially and not lapping with said pixel electrode selectively at least.
[Claim 6] Said 2nd conductive layer is an electro-optic device given in any 1 term of claims 1-5 characterized by connecting with a constant potential line electrically.
[Claim 7] An electro-optic device given in any 1 term of claims 1-6 characterized by having further the light-shielding film formed in said substrate side of a channel field through the substrate insulator layer at least among said semi-conductor layers.
[Claim 8] For said 1st conductive layer and said 2nd conductive layer, claims 1-7 characterized by including a refractory metal are electro-optic devices given in **** either.
[Claim 9] Said 2nd conductive layer and said data line are an electro-optic device given in any 1 term of claims 1-8 characterized by carrying out opposite arrangement selectively at least through an interlayer insulation film.
[Claim 10] An electro-optic device given in any 1 term of claims 1-9 characterized by having further the storage capacitance connected to said pixel electrode.
[Claim 11] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device according to claim 10 characterized by being prepared through an insulator layer on one electrode of said scanning line and said storage capacitance.
[Claim 12] The electro-optic device according to claim 11 which opposite arrangement of the 1st storage capacitance electrode which consists of said a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of said storage capacitance is carried out through the 1st dielectric film, and is characterized by carrying out opposite arrangement of the 3rd storage capacitance electrode which consists of a part of said 2nd storage capacitance electrode and said 1st conductive layer through the 2nd dielectric film, and forming said storage capacitance.
[Claim 13] Said 2nd conductive layer is an electro-optic device given in any 1 term of claims 10-12 characterized by connecting with said 2nd storage capacitance electrode.
[Claim 14] It is the electro-optic device according to claim 13 which said 2nd conductive layer is electrically connected to said 2nd storage capacitance electrode through the 4th contact hole, and is

characterized by said 4th contact hole being punctured by the same process as the process which punctures said 1st contact hole.
[Claim 15] Said 2nd storage capacitance electrode is an electro-optic device according to claim 12 which is installed and is characterized by being a capacity line.
[Claim 16] Said 2nd storage capacitance electrode is an electro-optic device according to claim 13 characterized by coming to connect with said light-shielding film.
[Claim 17] Said light-shielding film is an electro-optic device according to claim 16 which serves as a capacity line and is characterized by coming to connect it with said light-shielding film while said 2nd storage capacitance electrode is constituted by island shape for every elongation and pixel electrode along with said scanning line in between the data lines with which the flat-surface configuration on said substrate adjoins each other.
[Claim 18] For said 4th contact hole, said light-shielding film is an electro-optic device according to claim 15 characterized by connecting with said capacity line electrically through the 5th contact hole punctured by different flat-surface location.
[Claim 19] Said 2nd conductive layer and said light-shielding film are an electro-optic device given in any 1 term of claims 10-18 which it comes to connect electrically through said 2nd storage capacitance electrode, and are characterized by coming to connect said 2nd conductive layer and said light-shielding film with an adjoining pixel electrode.
[Claim 20] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device given in any 1 term of claims 1-19 characterized by being prepared in the lower layer rather than said data line.
[Claim 21] Said 2nd conductive layer is an electro-optic device given in any 1 term of ****** 1-20 characterized by specifying selectively at least the field which sees superficially, is established in island shape and met said data line among pixel opening fields.
[Claim 22] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device given in any 1 term of claims 1-10 characterized by being prepared in the upper layer rather than said data line.
[Claim 23] Said 2nd conductive layer is an electro-optic device according to claim 22 characterized by specifying the field which is prepared in the shape of a grid except for the field where it sees superficially and said 1st conductive layer exists, and met said data line and said scanning line of a pixel opening field.
[Claim 24] Said semi-conductor layer and said 1st conductive layer are an electro-optic device according to claim 22 or 23 characterized by connecting through the junction conductive layer which consists of the same film as said data line.
[Claim 25] It is the electro-optic device according to claim 24 which has the storage capacitance connected to said pixel electrode, and is characterized by ****(ing) said data line through an interlayer insulation film between one electrode of said storage capacitance, and said 2nd conductive layer.
[Claim 26] In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, The process which forms the 2nd conductive layer from the same film as the 1st conductive layer of protection-from-light nature, and said 1st conductive layer so that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd interlayer insulation film, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It is the manufacture approach of the electro-optic device characterized by being formed so that it may have the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer may be seen superficially and it may lap with said data line selectively at least.
[Claim 27] In the process which forms said data line after the process which forms said 2nd interlayer

insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer The manufacture approach of the electro-optic device according to claim 23 characterized by forming said 2nd conductive layer so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.

[Claim 28] In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd layer insulation gland at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The manufacture approach of the electro-optic device characterized by including the process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer.

[Claim 29] In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance at said 1st interlayer insulation film and said 2nd layer insulation gland at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer The manufacture approach of the electro-optic device according to claim 24 characterized by forming said 2nd conductive layer so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[Claim 30] Electronic equipment characterized by having the electro-optic device of a publication in any 1 term of claim 1 to claim 25.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of an electro-optic device and its manufacture approach, and belongs to an electro-optic device equipped with the conductive layer for the junction for taking an electric flow good especially between a pixel electrode and the thin film transistor for pixel switching (TFT being called suitably below Thin Film Transistor), and its manufacture approach list at the technical field of electronic equipment.
[0002]
[Description of the Prior Art] Conventionally, come to **** electrooptic material, such as liquid crystal, between the substrates of a couple, and this kind of electro-optic device to the TFT array substrate which is an example of one substrate Two or more pixel electrodes are prepared in the shape of a matrix, and to the opposite substrate which is an example of the substrate of another side In order to specify the pixel opening field (namely, field where light passes the electrooptic material part in each pixel) in each pixel, it is common that a light-shielding film is prepared in the shape of a grid corresponding to the gap of a pixel electrode. In this case, in order to make it the contrast ratio in a display image not fall by optical leakage around each pixel electrode, it is constituted so that it may see superficially and a grid-like light-shielding film may lap with each pixel electrode a little. Under the present circumstances, since especially the light-shielding film prepared in the opposite substrate side is comparatively separated from the pixel electrode through electrooptic material etc., in consideration of the lamination gap of light and both substrates which carries out incidence, it is necessary to put it aslant by the margin with remarkable pixel electrode and light-shielding film like ****. This serves as a big obstruction at the time of raising a pixel numerical aperture (namely, rate which the pixel opening field in each pixel occupies).
[0003] So, recently, under the general request of performing bright image display, in order to raise the pixel numerical aperture in each pixel, the technique of specifying each pixel opening field selectively is also generalized by only the protection-from-light gland by the side of an opposite substrate not prescribing a pixel opening field, but forming the data line broadly so that the clearance between the lengthwise directions of a pixel electrode may be covered from protection-from-light nature ingredients, such as aluminum (aluminum). According to this technique, since the data line prescribed the pixel opening field selectively, a pixel numerical aperture can be raised.
[0004] On the other hand, in this kind of electro-optic device, although it is necessary to connect mutually, each pixel electrode and switching elements, such as TFT prepared for example, in each pixel Since two or more interlayer insulation films for insulating electrically wiring and these of the scanning line, a capacity line, the data line, etc. mutually are included, for example, 1000nm (nano meter) extent or a thicker laminated structure than it exists among both, It becomes difficult to puncture the contact hole for connecting between both electrically.
[0005] Under a general request called high-definition-izing of the display image in this kind of electro-optic device, improvement in detailed-izing of a pixel pitch and a pixel numerical aperture, adequate supply of the picture signal to a pixel electrode, etc. become important.
[0006] However, since the data line and a pixel electrode have lapped selectively through the interlayer insulation film according to the technique of specifying a pixel opening field selectively with the data line mentioned above, if TFT prepared in each pixel is considered, according to the lap of the data line and the pixel electrode which were mentioned above, parasitic capacitance will arise between the source and a drain. Switching operation is carried out so that TFT to which a picture signal is supplied through

the data line generally [here] may make the fixed potential according to a picture signal hold to a pixel electrode for an one-frame period, but during this period, since it sways frequently to the potential of the picture signal supplied to TFT of an other bank, the electrical potential difference which TFT should carry out [an electrical potential difference] abnormality actuation and should be made to hold to a pixel electrode will leak the data line with the parasitic capacitance between the above-mentioned source and a drain. Consequently, supply of the picture signal to a pixel electrode becomes unstable, and while saying that degradation of a display image is caused eventually, there is ****.

[0007] On the other hand, under a general request called the simplification and low-cost-izing of an equipment configuration in this kind of electro-optic device, also in case a certain function is added or raised, it becomes important to use effectively not to make the conductive layer in a laminated structure or the number of insulator layers increase recklessly or one film in order to achieve two or more set ability.

[0008] This invention is made in view of an above-mentioned trouble, and it has the comparatively easy configuration, and a pixel numerical aperture is high and let it be a technical problem to offer the high-definition electro-optic device in which image display is possible and its high-definition manufacture approach.

[0009]

[Means for Solving the Problem] In order that the electro-optic device of this invention may solve the above-mentioned technical problem, to a substrate Two or more scanning lines, The thin film transistor and pixel electrode which have been arranged corresponding to the crossover of two or more data lines, and the said each scanning line and said each data line, The 1st conductive layer of the protection-from-light nature which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, and was connected to said semi-conductor layer and electric target, and was connected to said pixel electrode and electric target, It consists of the same film as said 1st conductive layer, and has the 2nd conductive layer which saw superficially and has lapped with said data line selectively at least.

[0010] According to the configuration of the electro-optic device of this invention, it intervenes between a semi-conductor layer and a pixel electrode, and connects with the semi-conductor layer and the electric target by one side, and the 1st conductive layer is another side and is connected to the pixel electrode and the electric target. Therefore, the 1st conductive layer becomes possible [avoiding the difficulty in the case of functioning as a conductive layer for the junction for connecting electrically a pixel electrode and the drain field of a semi-conductor layer, for example, carrying out direct continuation of between both through one contact hole].

[0011] Moreover, since the 2nd conductive layer was seen superficially and has lapped with said data line selectively at least, it becomes possible [carrying out the redundancy of the protection from light of each pixel by the 2nd conductive layer in addition to the data line].

[0012] In the mode of 1 of the electro-optic device of this invention, said 2nd conductive layer was seen superficially and has lapped with said pixel electrode selectively at least.

[0013] According to this configuration, especially the 2nd conductive layer formed between the pixel electrodes which see superficially and adjoin selectively at least has lapped with the pixel electrode. For this reason, the 2nd conductive layer part which lapped with this pixel electrode selectively can prescribe the pixel opening field in each pixel selectively at least. Under the present circumstances, especially in the part where the pixel opening field was specified by the 2nd conductive layer, since it sees superficially and there is no clearance between a pixel electrode and the 2nd conductive layer, the optical leakage through such a clearance does not take place. Consequently, eventually, a contrast ratio is raised. Since the data line does not need to prescribe a pixel opening field like before, it becomes unnecessary simultaneously, to pile up the data line and a pixel electrode in the part where the pixel opening field was specified by the 2nd conductive layer. Consequently, it is not necessary to generate the parasitic capacitance between the sources of a thin film transistor and the drains in each pixel according to the structure where the data line and a pixel electrode lap through an interlayer insulation film. For this reason, it originates in the potential shake concerned of the data line which sways frequently to the potential of the picture signal supplied in predetermined periods, such as one etc. frame, at the thin film transistor of an other bank, a thin film transistor carries out abnormality actuation with the parasitic capacitance between the above-mentioned source and a drain, and the situation which the electrical potential difference which should be made to hold to a pixel electrode leaks can be prevented. That is, switching operation of the thin film transistor is carried out, it can supply a picture

signal adequately to a pixel electrode through the data line and a thin film transistor, and, eventually, high definition-ization of a display image of it is attained by reduction of a flicker or line nonuniformity so that the fixed potential according to a picture signal may be made to hold to a pixel electrode.
[0014] Furthermore, since the function to specify a pixel opening field is given closing adequate supply of a picture signal to it if to the 2nd conductive layer which consists of the same film as this 1st conductive layer while giving the function to relay a thin film transistor and a pixel electrode to the 1st conductive layer, low cost-ization can be attained in the simplification list of a laminated structure and a manufacture process as a whole.
[0015] In other modes of the electro-optic device of this invention, it connects electrically through said semi-conductor layer and 1st contact hole, and said 1st conductive layer is electrically connected through said pixel electrode and 2nd contact hole.
[0016] According to this configuration, as compared with the case where one contact hole is punctured, the path of a contact hole can be made small from a pixel electrode to the drain field of a semi-conductor layer. That is, in order that etching precision may fall, in order to prevent the thrust omission in a thin semi-conductor layer, the dry etching which can make the path of a contact hole small must be suspended on the way, a process must be constructed so that it may puncture to a semi-conductor layer by wet etching eventually, and the path of a contact hole cannot but spread by wet etching without directivity, so that a contact hole is generally punctured deeply. On the other hand, in this mode, since what is necessary is just to connect between semi-conductor layers with a pixel electrode by the 1st and 2nd two in-series contact holes, it becomes possible to shorten distance which becomes possible [puncturing each contact hole by dry etching], or is punctured by wet etching at least. Consequently, the path of each contact hole can be made small, respectively, and flattening in the pixel electrode section located above the 1st or 2nd contact hole is promoted.
[0017] According to other modes of the electro-optic device of this invention, said data line is electrically connected through said semi-conductor layer and 3rd contact hole.
[0018] According to this configuration, the electric connection between the data line and the source field of a semi-conductor layer is obtained good through the 3rd contact hole.
[0019] According to other modes of the electro-optic device of this invention, said data line is seen superficially and does not lap with said pixel electrode selectively at least.
[0020] According to this configuration, by forming so that the data line and a pixel electrode may not lap as much as possible, it compares with the case where the data line and a pixel electrode are piled up, and the parasitic capacitance between the data line and a pixel electrode can be reduced certainly. Therefore, the electrical potential difference especially in a pixel electrode is stabilized, and a flicker and line nonuniformity can be reduced.
[0021] furthermore, the part with which the data line and a pixel electrode lapped through the interlayer insulation film -- it can be, generating of defects, such as an electric short circuit between both with high possibility of generating (short circuit), can be suppressed, and decline in the rate of an equipment defect and improvement in the yield at the time of manufacture are achieved eventually.
[0022] Other mode ****** of the electro-optic device of this invention and said 2nd conductive layer are electrically connected to the constant potential line.
[0023] According to this configuration, some parasitic capacitance is attached between the pixel electrode and the 2nd conductive layer which have lapped with the part at least, but the potential of the 2nd conductive layer is maintained at constant potential. for this reason, the adverse effect which potential fluctuation of the 2nd conductive layer has on the potential of a pixel electrode through the parasitic capacitance between a pixel electrode and the 2nd conductive layer -- it can decrease -- a pixel electrode -- the electrical potential difference to kick is stabilized more and a flicker and line nonuniformity can be reduced further.
[0024] According to other modes of the electro-optic device of this invention, it has further the light-shielding film formed in said substrate side of a channel field through the substrate insulator layer at least among said semi-conductor layers.
[0025] According to this configuration, the channel field to the light from a TFT array substrate side can be shaded by the light-shielding film formed in the substrate side of a channel field through the substrate insulator layer at least among semi-conductor layers. For this reason, high-definition image display becomes possible, reducing the optical leak in a channel field which originates in the optical exposure to thin film transistors, such as incident light, the rear-face reflected light, and the reflected light, and is generated at the time of actuation of the electro-optic device concerned, and reducing property change

and degradation of a thin film transistor.
[0026] According to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer contain a refractory metal.
[0027] according to this configuration -- ******** and an arrow -- two conductive layer consists of the metal simple substance containing at least one of Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), Mo (molybdenum), and Pb(s) (lead), an alloy, metal silicide, etc. For this reason, by high temperature processing in the various processes performed after the 1st conductive layer and the 2nd conductive layer formation in a manufacture process, the 1st conductive layer and the 2nd conductive layer concerned deform, or do not break.
[0028] According to other modes of the electro-optic device of this invention, opposite arrangement of said 2nd conductive layer and said data line is selectively carried out at least through an interlayer insulation film.
[0029] according to this configuration, but [not between the pixel electrodes with which potential is changed according to the picture signal which should be held] between the 2nd conductive layer by which potential was stabilized more, since capacity is added to the data line, it is possible to make it increase moderately, making it not cause the potential shake of the data line -- HI -- ** Even if it makes especially a pixel pitch detailed and makes data-line width of face detailed in connection with this, by making the capacity between the 2nd conductive layer increase, the lack of capacity of the data line can be suppressed and the write-in deficiency in performance in supply to the pixel electrode of the picture signal through the data line concerned can be prevented.
[0030] According to other modes of the electro-optic device of this invention, it has further the storage capacitance connected to said pixel electrode.
[0031] According to this configuration, the electrical-potential-difference holding time of the picture signal in a pixel electrode can be lengthened far, and storage capacitance raises a contrast ratio very efficiently.
[0032] In this mode, said 1st conductive layer and 2nd conductive layer may be prepared through an insulator layer on one electrode of said scanning line and said storage capacitance.
[0033] According to this configuration, by the 2nd conductive layer possible [a pixel electrode and a semi-conductor layer] and prepared through the insulator layer on one electrode of the scanning line and storage capacitance, the 1st conductive layer prepared through the insulator layer on one electrode of the scanning line and storage capacitance can prescribe a pixel opening field, and a configuration becomes possible simply about capacity between the 2nd conductive layer and one electrode of storage capacitance further.
[0034] In the mode further equipped with this storage capacitance, opposite arrangement of the 1st storage capacitance electrode which consists of said a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of said storage capacitance is carried out through the 1st dielectric film, opposite arrangement of the 3rd storage capacitance electrode which consists of a part of said 2nd storage capacitance electrode and said 1st conductive layer may be carried out through the 2nd dielectric film which is said insulator layer, and said storage capacitance may be formed.
[0035] According to this configuration, opposite arrangement of the 1st storage capacitance electrode which consists of a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of storage capacitance is carried out through the 1st dielectric film, the 1st storage capacitance is constituted, opposite arrangement of the 3rd storage capacitance electrode which consists of a part of 2nd storage capacitance electrode and 1st conductive layer is carried out through the 2nd dielectric film on the other hand, and the 2nd storage capacitance is constituted. And since storage capacitance is formed in each pixel electrode from these 1st and 2nd storage capacitance, a non-pixel opening field is used effectively and, moreover, comparatively mass storage capacitance can be built using three-dimensional structure.
[0036] Said 2nd conductive layer may be connected to said 2nd storage capacitance electrode in the mode further equipped with this storage capacitance.
[0037] According to this configuration, some parasitic capacitance is attached between the pixel electrode and the 2nd conductive layer which have lapped selectively at least, but the potential of the 2nd conductive layer is maintained at the potential of the 2nd storage capacitance electrode.
[0038] Thus, when connecting the 2nd conductive layer to the 2nd storage capacitance electrode, said 2nd conductive layer is connected to said 2nd storage capacitance electrode through the 4th contact hole, and said 4th contact hole may be punctured by the same process as the process which punctures said 1st

contact hole.
[0039] According to this configuration, since the 2nd conductive layer can be connected to the 2nd storage capacitance electrode comparatively easily and the 4th contact hole is punctured to puncturing the 1st contact hole moreover and coincidence, it is useful to the simplification of a manufacture process.

[0040] The 2nd storage capacitance electrode here is built and is good also as a capacity line.
[0041] According to this configuration, a capacity line is made into constant potential, or it is large capacity at least, and that potential fluctuation is small. For this reason, the adverse effect which potential fluctuation of the 2nd conductive layer has on the potential of a pixel electrode can be reduced through the parasitic capacitance between a pixel electrode and the 2nd conductive layer.
[0042] This 2nd storage capacitance electrode may be connected with ******.
[0043] According to this configuration, potential of the 2nd storage capacitance electrode and a light-shielding film can be made the same, and if the configuration which makes predetermined potential either the 2nd storage capacitance electrode and protection-from-light gland is taken, potential of another side will also be made with predetermined potential. Consequently, the adverse effect by the potential shake in the 2nd storage capacitance electrode or a light-shielding film can be reduced. Moreover, wiring and the capacity line which consist of a light-shielding film can be mutually operated as redundancy wiring.
[0044] This light-shielding film serves as a capacity line, and said 2nd storage capacitance electrode may be connected to said light-shielding film while it is constituted by island shape for every elongation and pixel electrode along with said scanning line in between the data lines with which the flat-surface configuration on said substrate adjoins each other.
[0045] According to this configuration, since the 2nd storage capacitance electrode can be constituted in island shape for every pixel electrode, a pixel numerical aperture can be raised. Moreover, the 2nd storage capacitance can also be made redundancy wiring of a capacity line with wiring, then a light-shielding film.
[0046] Furthermore, said light-shielding film may be electrically connected to said capacity line through the 5th contact hole punctured by different flat-surface location from said 4th contact hole.
[0047] According to this configuration, the channel field to the light from a substrate side can be shaded by the light-shielding film formed in the substrate side of a channel field through the substrate insulator layer at least among semi-conductor layers. And a light-shielding film is conductivity, and since it connects with the capacity line through the 5th contact hole, it becomes possible to operate a light-shielding film of it as redundancy wiring of a capacity line, and, eventually, it can attain high definition-ization of a display image by stabilizing the potential of a capacity line more by attaining low resistance-ization of a capacity line. Moreover, the 4th contact hole and the 5th contact hole can prevent the faulty connection in the 4th contact hole and the 5th contact hole by forming in a different flat-surface location.

[0048] Furthermore, it may come to connect said 2nd conductive layer and said light-shielding film electrically through said 2nd storage capacitance electrode, and said 2nd conductive layer and said light-shielding film may be connected to the adjoining pixel electrode.
[0049] According to this configuration, the 2nd conductive layer can be used as a capacity line. Moreover, by making the 2nd storage capacitance electrode into a capacity line, and connecting the 2nd conductive layer and the 2nd storage capacitance electrode, it can be double, a capacity line can be formed and redundant structure can be realized.
[0050] According to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer are prepared in the lower layer rather than said data line.
[0051] According to this configuration, by the 2nd conductive layer possible [a pixel electrode and a semi-conductor layer] and prepared in the lower layer rather than the data line, the 1st conductive layer prepared in the lower layer can prescribe a pixel opening field, and a configuration becomes possible from the data line simply about capacity between the 1st conductive layer and the 2nd storage capacitance electrode further.
[0052] According to other modes of the electro-optic device of this invention, said 2nd conductive layer is seen superficially, is prepared in island shape, and specifies selectively at least the field which met said data line among pixel opening fields.
[0053] According to this configuration, the 2nd conductive layer which saw superficially and was prepared in island shape can prescribe selectively at least the field which met the data line among pixel

opening fields. For example, the 2nd conductive layer can be formed in the field of most except the field where the contact hole which connects the channel field, the data line, and the semi-conductor layer of a thin film transistor among the pixel opening fields which met the data line was punctured, and it is possible to specify the pixel opening field in the field of this most by the 2nd conductive layer concerned.

[0054] Or according to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer are characterized by being prepared as a layer further than said data line from said substrate (i.e., the upper layer).

[0055] According to this configuration, the 2nd conductive layer which junction of a pixel electrode and a semi-conductor layer is possible, and was prepared in the upper layer rather than the data line by the 1st conductive layer prepared as a layer further than the data line from a substrate can prescribe a pixel opening field. In this case, especially, the 2nd conductive layer may be prepared in all the fields on the data line through an interlayer insulation film, and may be prepared through an interlayer insulation film on the scanning line. Moreover, since the location of the contact hole which connects the 1st conductive layer and a pixel electrode can be set as the location of arbitration if it is in a non-opening field, it increases [a design degree of freedom] and is advantageous.

[0056] Said 2nd conductive layer is prepared in the shape of [said] a grid except for the field where it sees superficially and said 1st conductive layer exists, and it may consist of this mode so that the field which met said data line and said scanning line of a pixel opening field, respectively may be specified.

[0057] According to this configuration, since it is prepared in the shape of a grid except for the field where the 1st conductive layer exists, the 2nd conductive layer can specify the field met, respectively to the data line and the scanning line of a pixel opening field, i.e., also specify all the profiles of a pixel opening field. In addition, about the gap of the 1st conductive layer and the 2nd conductive layer, optical leakage can be easily prevented by the light-shielding film by the side of an opposite substrate, the thin film transistor of the thin film transistor bottom, the installation part of the data line, etc., for example.

[0058] In the mode by which this 1st conductive layer and 2nd conductive layer were prepared in the upper layer, said semi-conductor layer and said 1st conductive layer may be connected through the junction conductive layer which consists of the same film as said data line.

[0059] Since according to this configuration from a pixel electrode to the junction conductive layer which consists of the same layer as the data line is connected electrically and even the semi-conductor layer was further connected electrically by this junction conductive layer rather than the data line by the 1st conductive layer prepared in the upper layer, junction becomes possible good about from a pixel electrode to a semi-conductor layer by the 1st conductive layer and junction conductive layer which are two conductive layers for junction. Also when the electric affinity of aluminum film which constitutes especially the data line, and the ITO (Indium Tin Oxide) film which constitutes a pixel electrode is bad, it is advantageous to these both and an electric target at the point which should just form the 1st conductive layer from a congenial ingredient (for example, refractory metal).

[0060] In the mode by which this 1st conductive layer and 2nd conductive layer are prepared in the upper layer, it has the storage capacitance connected to said pixel electrode, and said data line may be ****(ed) through an interlayer insulation film between one electrode of said storage capacitance, and said 2nd conductive layer.

[0061] According to this configuration, but [not between the pixel electrodes with which potential is changed according to the picture signal which should be held] between one electrodes of the 2nd conductive layer by which potential was stabilized more, and storage capacitance, since capacity can be made to add to the data line, it becomes possible to make the capacity of the data line increase moderately, making it not cause a potential shake. Even if it makes especially a pixel pitch detailed and makes data-line width of face detailed in connection with this, by making the capacity between the 2nd conductive layer and the 2nd storage capacitance electrode increase, the lack of capacity of the data line can be suppressed and the write-in deficiency in performance in supply to the pixel electrode of the picture signal through the data line concerned can be prevented.

[0062] In order that the manufacture approach of the 1st electro-optic device of this invention may solve the above-mentioned technical problem In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film

on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance in the predetermined field on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures ** 1 contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, So that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 2nd insulator layer The 1st conductive layer of protection-from-light nature, The process which forms the 2nd conductive layer from the same film as said 1st conductive layer, and the process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd **********, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It has the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer is formed so that it may see superficially and may lap with said data line selectively at least.

[0063] According to the manufacture approach of the 1st electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the 1st contact hole which leads to a semi-conductor layer is punctured by an insulating thin film and the 1st interlayer insulation film, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a semi-conductor layer electrically through this 1st contact hole. The 2nd conductive layer is formed so that it may be selectively arranged at least in the gap of the field in which it sees superficially and a pixel electrode is simultaneously formed from the same film as this 1st conductive layer. Then, laminating formation of the 2nd interlayer insulation film, the data line, and the 3rd interlayer insulation film is carried out in this order. Next, the 2nd contact hole which leads to the 1st conductive layer is punctured, and pixel ionization formation is carried out so that it may connect with the 1st conductive layer electrically through this 2nd contact hole. Therefore, the electro-optic device of this invention which has the configuration which forms the 1st and 2nd conductive layers as a layer near a substrate, and relays a pixel electrode and a semi-conductor layer by the 2nd conductive layer through two contact holes rather than the data line mentioned above can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[0064] In the mode of 1 of the manufacture approach of the 1st electro-optic device of this invention In the process which forms said data line after the process which forms said 2nd interlayer insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.

[0065] According to this configuration, the 3rd contact hole which leads to a semi-conductor layer is punctured after formation of the 2nd interlayer insulation film, and the data line is formed so that it may connect with a semi-conductor layer electrically through this 3rd contact hole. Furthermore, the 4th contact hole which leads to one electrode of storage capacitance simultaneously at the time of puncturing of the 1st contact hole is punctured, and the 2nd conductive layer is formed so that it may connect with one electrode of storage capacitance electrically through this 4th contact hole. Therefore, the electro-optic device of this invention which has the configuration to which the data line and the semi-conductor layer which were mentioned above are electrically connected to through the contact hole, and the 2nd conductive layer and one electrode of storage capacitance were electrically connected through the contact hole can be manufactured comparatively easily. Since these two contact holes are punctured especially simultaneously, low cost-ization can be attained in the simplification list of a manufacture process.

[0066] In order that the manufacture approach of the 2nd electro-optic device of this invention may solve the above-mentioned technical problem In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor

were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, It is characterized by including the process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer.

[0067] According to the manufacture approach of the 2nd electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the contact hole which leads to a semi-conductor layer is punctured, and a junction conductive layer is formed from the same film as the data line so that it may connect with a semi-conductor layer electrically, at the same time the data line is formed. Next, after the 2nd interlayer insulation film is formed, the contact hole which leads to a junction conductive layer is punctured, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a junction conductive layer electrically. It can come, simultaneously the 2nd conductive layer is formed from the same film as the 1st conductive layer. Then, the 3rd interlayer insulation film is formed, the contact hole which leads to the 1st conductive layer is punctured, and a pixel electrode is formed so that it may connect with the 1st conductive layer electrically. Therefore, as the layer further than the data line from a substrate, i.e., the upper layer, while forming a junction conductive layer as a conductive layer which consists of the same film as the data line mentioned above, the 1st conductive layer is formed, and while relaying a pixel electrode and a semi-conductor layer by the junction conductive layer and the 1st conductive layer through three contact holes, the electro-optic device of this invention which has the configuration which specifies a pixel opening field by the 2nd conductive layer can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[0068] In the mode of 1 of the manufacture approach of the 2nd electro-optic device of this invention In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film and said 2nd interlayer insulation film at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[0069] According to this mode, the 4th contact hole which leads to a semi-conductor layer is punctured after formation of the 1st interlayer insulation film, and the data line is formed so that it may connect with a semi-conductor layer electrically. Furthermore, when puncturing a contact hole to the 2nd interlayer insulation film, the contact hole which leads to one electrode of storage capacitance simultaneously is punctured, and the 3rd conductive layer is formed so that it may connect with one electrode of storage capacitance electrically. Therefore, the electro-optic device of this invention which has the configuration to which the data line and the semi-conductor layer which were mentioned above are electrically connected to through the contact hole, and the 2nd conductive layer and one electrode of

storage capacitance were electrically connected through the contact hole can be manufactured comparatively easily. Since these two contact holes are punctured especially simultaneously, low cost-ization can be attained in the simplification list of a manufacture process.
[0070] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[0071]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing.
[0072] (The 1st operation gestalt) The configuration of the electro-optic device in the 1st operation gestalt of this invention is explained with reference to drawing 4 from drawing 1 . Drawing 1 is equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring, drawing 2 is a top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 3 is the A-A' sectional view of drawing 2 , and drawing 4 is B-B of drawing 2 , and a sectional view. In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for each class or every each part material in drawing 3 and drawing 4 .
[0073] In drawing 1 , two or more formation of TFT30 for two or more pixels formed in the shape of [which constitutes the image display field of the electro-optic device in this operation gestalt] a matrix to control pixel electrode 9a corresponding to the crossover of scanning-line 3a and data-line 6a is carried out at the shape of a matrix, and data-line 6a to which a picture signal is supplied is electrically connected to the source concerned of TFT30. The picture signals Sl, S2, --, Sn written in data-line 6a may be supplied to line sequential, and you may make it supply them to this order for every group to two or more data-line 6a which adjoin each other. Moreover, scanning-line 3a is electrically connected to the gate of TFT30, and it consists of predetermined timing so that the scan signals Gl, G2, --, Gm may be impressed to scanning-line 3a in pulse line sequential at this order. It connects with the drain of TFT30 electrically, and pixel electrode 9a writes in the picture signals Sl and S2 supplied from data-line 6a in TFT30 which is a switching element when only a fixed period closes the switch, ---, and Sn to predetermined timing. Fixed period maintenance of the picture signals Sl, S2, --, Sn of the predetermined level written in liquid crystal as an example of electrooptic material through pixel electrode 9a is carried out between the counterelectrodes (it mentions later) formed in the opposite substrate (it mentions later). When the orientation and order of molecular association change with the voltage levels impressed, liquid crystal modulates light and enables a gradation display. According to the electrical potential difference impressed when it was in no MARI White mode, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from an electro-optic device as a whole. Here, storage capacitance 70 is added to the liquid crystal capacity and juxtaposition which are formed [that the held picture signal leaks and] between pixel electrode 9a and a counterelectrode at a **** sake. For example, as for the electrical potential difference of pixel electrode 9a, only time amount also with triple figures longer than the time amount to which the picture signal was impressed is held with storage capacitance 70 at the source of TFT30. Thereby, it is improved further and a maintenance property can realize the high electro-optic device of a contrast ratio.
[0074] In drawing 2 , on the TFT array substrate of an electro-optic device, two or more transparent pixel electrode 9a (the profile is shown by dotted-line section 9a') is prepared in the shape of a matrix, and data-line 6a, scanning-line 3a, and capacity line 3b are prepared respectively along the boundary of pixel electrode 9a in every direction. Data-line 6a is electrically connected to the below-mentioned source field through the contact hole 5 among semi-conductor layer 1a which a metaphor becomes from the polish recon film. Island-shape 1st conductive layer (1st barrier layer is called hereafter) 80a and 2nd conductive layer (2nd barrier layer is called hereafter) 80b are prepared in the field (field shown with the slash of a drawing Nakamigi riser) in alignment with field and data-line 6a in alignment with scanning-line 3a in the gap between pixel electrode 9a which adjoin each other, respectively. Especially with this operation gestalt, 1st barrier layer 80a and 2nd barrier layer 80b are formed from the electric conduction film of the same protection-from-light nature. Pixel electrode 9a relays 1st barrier layer 80a, and is electrically connected to the contact hole 8a list to the below-mentioned drain field among semi-conductor layer 1a through contact hole 8b. Capacity line 3b is electrically connected to 2nd barrier

layer 80b through contact hole 8c. Moreover, scanning-line 3a is arranged so that the lower right in drawing may counter channel field 1a' shown in the slash field of ** among semi-conductor layer 1a, and scanning-line 3a functions as a gate electrode. Thus, TFT30 for pixel switching by which opposite arrangement of the scanning-line 3a was carried out as a gate electrode is formed in the crossing part of scanning-line 3a and data-line 6a at channel field 1a', respectively.
[0075] Capacity line 3b has the main track section mostly extended in the shape of a straight line along with scanning-line 3a, and the lobe which projected along with data-line 6a from the part which intersects data-line 6a.
[0076] Contact hole 8a connects with the drain field of semi-conductor layer 1a electrically, contact hole 8b connects with pixel electrode 9a electrically, and especially 1st barrier layer 80a is functioning as a buffer between the drain field of semi-conductor layer 1a, and pixel electrode 9a, respectively. Contact hole 8b is behind explained in full detail in this 1st barrier layer 80a and a contact hole 8a list.
[0077] Moreover, 1st light-shielding film 11a may be prepared in the field shown by the thick wire in drawing, respectively so that it may pass along scanning-line 3a, capacity line 3b, and the TFT30 bottom. Respectively, 1st light-shielding film 11a is good for the part which intersects data-line 6a to form in the method of drawing Nakashita broadly, to see channel field 1a' of TFT30 for pixel switching from a TFT array substrate side by this broad part, and to make it prepare in a wrap location, respectively while forming it in the shape of stripes along with scanning-line 3a.
[0078] Next, as shown in the sectional view of drawing 3 , the electro-optic device is equipped with the TFT array substrate 10 which constitutes an example of the substrate of while it is transparence, and the opposite substrate 20 which it is the transparence by which opposite arrangement is carried out at this, and also constitutes an example of the substrate of a way. The TFT array substrate 10 consists of for example, a quartz substrate, a glass substrate, and a silicon substrate, and the opposite substrate 20 consists of a glass substrate or a quartz substrate. Pixel electrode 9a is prepared in the TFT array substrate 10, and the orientation film 16 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the upside. Pixel electrode 9a consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 16 consists of organic thin films, such as for example, a polyimide thin film.
[0079] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film.
[0080] TFT30 for pixel switching which carries out switching control of each pixel electrode 9a is formed in the location which adjoins each pixel electrode 9a at the TFT array substrate 10.
[0081] As further shown in the opposite substrate 20 at drawing 3 , the 2nd light-shielding film 23 is formed in the non-opening field of each pixel. For this reason, incident light does not invade into channel field 1a' of semi-conductor layer 1a of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c from the opposite substrate 20 side. Furthermore, the 2nd light-shielding film 23 has functions, such as color mixture prevention of the color material at the time of forming improvement in contrast and a light filter.
[0082] Thus, it is constituted, and between the TFT array substrates 10 and the opposite substrates 20 which have been arranged so that pixel electrode 9a and a counterelectrode 21 may meet, the liquid crystal which is an example of electrooptic material is enclosed with the space surrounded by the below-mentioned sealant, and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 16 and 22 in the condition that the electric field from pixel electrode 9a are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant may stick the TFT array substrate 10 and the opposite substrate 20 around those, and gap material, such as glass fiber for making distance between both substrates into a predetermined value or a glass bead, is mixed.
[0083] Furthermore, as shown in drawing 3 , in the location which counters TFT30 for pixel switching respectively, it is good between the TFT array substrate 10 and each TFT30 for pixel switching to prepare 1st light-shielding film 11a. 1st light-shielding film 11a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are a desirable opaque refractory metal, an alloy, metal silicide, etc. If constituted from such an ingredient, 1st light-shielding film 11a is destroyed

by high temperature processing in the formation process of TFT30 for pixel switching performed after the formation process of 1st light-shielding film 11a on the TFT array substrate 10, or it can avoid fusing by it. Since 1st light-shielding film 11a is formed, the situation in which the reflected light (return light) from the TFT array substrate 10 side etc. carries out incidence to channel field 1a' of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c can be prevented, and the property of TFT30 for pixel switching does not change with generating of the current by the light resulting from this, or it does not deteriorate.

[0084] In addition, 1st light-shielding film 11a formed in the shape of stripes may be installed for example, in the bottom of scanning-line 3a, and may be electrically connected to a constant potential line. Thus, if constituted, potential fluctuation of 1st light-shielding film 11a will not have an adverse effect on 1st light-shielding film 11a to TFT30 for pixel switching by which opposite arrangement is carried out. In this case, the constant potential line supplied to constant potential lines, such as a negative supply supplied to the circumference circuits (for example, a scanning-line actuation circuit, a data-line actuation circuit, etc.) for driving the electro-optic device concerned as a constant potential line and a positive supply, a touch-down power source, and a counterelectrode 21 is mentioned. In addition, 1st light-shielding film 11a may be formed by the shape of a grid along with data-line 6a and scanning-line 3a, and it may be formed in island shape so that channel field 1a' of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c may be covered at least.

[0085] Furthermore, the substrate insulator layer 12 is formed between 1st light-shielding film 11a and two or more TFT30 for pixel switching. The substrate insulator layer 12 is formed in order to insulate electrically semi-conductor layer 1a which constitutes TFT30 for pixel switching from 1st light-shielding film 11a. Furthermore, the substrate insulator layer 12 also has a function as substrate film for TFT30 for pixel switching by being formed all over the TFT array substrate 10. That is, it has the function to prevent degradation of the property of TFT30 for pixel switching with the dry area at the time of polish of the front face of the TFT array substrate 10, the dirt which remains after washing. The substrate insulator layer 12 consists of high insulation glass, such as NSG (non doped silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), or an oxidation silicone film, a silicon nitride film, etc. The substrate insulator layer 12 can also protect the situation where 1st light-shielding film 11a pollutes the TFT30 grade for pixel switching.

[0086] 1st storage capacitance 70a is constituted by considering as the 1st dielectric film which considered as the 1f of the 1st storage capacitance electrodes, used as the 2nd storage capacitance electrode a part of capacity line 3b which counters this, installed [semi-conductor layer 1a was installed from high concentration drain field 1e, and] the insulating thin film 2 containing gate dielectric film with this operation gestalt from the location which counters scanning-line 3a, and was pinched by inter-electrode [these]. Furthermore, a part of this 2nd storage capacitance electrode and 1st barrier layer 80a which counters are used as the 3rd storage capacitance electrode, and the 1st interlayer insulation film 81 is formed in inter-electrode [these]. The 1st interlayer insulation film 81 functions as the 2nd dielectric film, and 2nd storage capacitance 70b is formed. And parallel connection of these 1st storage capacitance 70a and the 2nd are recording **** 70b is carried out through contact hole 8a, and storage capacitance 70 is constituted. Since especially the insulating thin film 2 as the 1st dielectric film of 1st storage capacitance 70a is exactly gate dielectric film of TFT30 formed on the polish recon film of high temperature oxidation, it can be thinly made into the insulator layer of high pressure-proofing, and can constitute 1st storage capacitance 70a from small area as mass storage capacitance comparatively. Moreover, since the 1st interlayer insulation film 81 can also be formed more thinly than the insulating thin film 2 as well as [or] the insulating thin film 2, 2nd storage capacitance 70b can constitute it as storage capacitance mass in small area comparatively. Therefore, let storage capacitance 70 which consists of these 1st storage capacitance 70a and 2nd storage capacitance 70b in three dimensions be storage capacitance mass in small area, using effectively the tooth space which separated from a pixel opening field called the field (namely, field in which capacity line 3b was formed) which the disclination of liquid crystal generates along with the field under data-line 6a, and scanning-line 3a.

[0087] Thus, an oxidation silicone film, a silicon nitride film, etc. are sufficient as the 1st interlayer insulation film 81 which constitutes 2nd storage capacitance 70b, and it may consist of multilayers. The 1st interlayer insulation film 81 can be formed with various kinds of well-known techniques (a reduced pressure CVD method, a plasma-CVD method, the oxidizing [thermally] method, etc.) used for generally forming the insulating thin films 2, such as gate dielectric film. Since the path of contact hole 8a can be made still smaller by forming the 1st interlayer insulation film 81 thinly, the hollow and

irregularity of 1st barrier layer 80a in contact hole 8a mentioned above are still smaller, it ends, and flattening in pixel electrode 9a located in the upper part is promoted further.
[0088] In drawing 3 TFT30 for pixel switching It has LDD (Lightly Doped Drain) structure. Channel field 1a' of semi-conductor layer 1a in which a channel is formed of the electric field from scanning-line 3a and concerned scanning-line 3a, 1d list of high concentration source fields of low concentration source field 1b of the insulating thin film 2 containing the gate dielectric film with which scanning-line 3a and semi-conductor layer 1a are insulated, data-line 6a, and semi-conductor layer 1a and low concentration drain field 1c, and semi-conductor layer 1a is equipped with high concentration drain field 1e. One to which it corresponds of two or more pixel electrode 9a relays 1st barrier layer 80a to high concentration drain field 1e, and it is electrically connected to it. Low concentration drain field 1c and high concentration drain field 1e are formed in low concentration source field 1b and 1d list of high concentration source fields to semi-conductor layer 1a like the after-mentioned by doping the impurity the object for n molds of predetermined concentration, or for p molds according to whether the channel of n mold or p mold is formed. TFT of an n-type channel has the advantage that working speed is quick, and it is used as TFT30 for pixel switching which is the switching element of a pixel in many cases. this operation gestalt -- especially -- data-line 6a -- low [, such as aluminum,] -- it consists of protection-from-light nature and conductive thin films, such as metal membrane metallurgy group silicide [****]. [, such as alloy film,] Moreover, on 1st barrier layer 80a and the 1st interlayer insulation film 81, the 2nd interlayer insulation film 4 with which contact hole 8b which leads to the contact hole 5 and 1st barrier layer 80a which lead to 1d of high concentration source fields was formed respectively is formed. Data-line 6a is electrically connected to 1d of high concentration source fields through the 1d [of this high concentration source field] contact hole 5. Furthermore, on data-line 6a and the 2nd interlayer insulation film 4, the 3rd interlayer insulation film 7 with which contact hole 8b to 1st barrier layer 80a was formed is formed. Through this contact hole 8b, it connects with 1st barrier layer 80a electrically, and pixel electrode 9a relays 1st barrier layer 80a further, and is electrically connected to high concentration drain field 1e through contact hole 8a. The above-mentioned pixel electrode 9a is prepared in the top face of the 3rd interlayer insulation film 7 constituted in this way.
[0089] Although TFT30 for pixel switching has LDD structure as mentioned above preferably, it may be TFT of the self aryne mold which may have the offset structure which does not drive an impurity into low concentration source field 1b and low concentration drain field 1c, drives in an impurity by high concentration by using as a mask the gate electrode which consists of a part of scanning-line 3a, and forms the high concentration source and a drain field in self align.
[0090] Moreover, although considered as the single gate structure which has arranged one gate electrode of TFT30 for pixel switching among 1d [of high concentration source fields], and high concentration drain field 1e with this operation gestalt, two or more gate electrodes may be arranged among these. Under the present circumstances, to each gate electrode, the same signal is made to be impressed. Thus, if TFT is constituted above the dual gate or the triple gate, the leakage current of a joint with a channel, the source, and a drain field can be prevented, and the current at the time of OFF can be reduced. If at least one of these gate electrodes is made into LDD structure or offset structure, the OFF state current can be reduced further and the stable switching element can be obtained.
[0091] As shown in drawing 2 and drawing 3 , since high concentration drain field 1e and pixel electrode 9a are electrically connected via 1st barrier layer 80a through contact hole 8a and contact hole 8b, in the electro-optic device of this operation gestalt, the path of contact hole 8a and contact hole 8b can be made small from pixel electrode 9a to a drain field as compared with the case where one contact hole is punctured, respectively. That is, etching precision must suspend the dry etching which can make the path of a contact hole small on the way, and when puncturing one contact hole, in order to fall (for example, in order to prevent the thrust omission in about 50nm very thin semi-conductor layer 1a), it must construct a process so that it may puncture to semi-conductor layer 1a by wet etching eventually, so that a contact hole is punctured deeply. Or it will be necessary to be based on dry etching, to run and to prepare the polish recon film for prevention separately.
[0092] On the other hand, with this operation gestalt, since what is necessary is just to connect pixel electrode 9a and high concentration drain field 1e by two in-series contact hole 8a and contact hole 8b, it becomes possible to puncture these contact hole 8a and contact hole 8b by dry etching, respectively. Or it becomes possible to shorten distance punctured by wet etching at least. However, in order to attach some taper to contact hole 8a and contact hole 8b, it may dare to be made to perform short-time wet etching after dry etching comparatively.

[0093] Since the hollow and irregularity which the path of contact hole 8a and contact hole 8b can be made small, respectively, and are formed in the front face of 1st barrier layer 80a in contact hole 8a are also small and end according to this operation gestalt as mentioned above, flattening in the part of pixel electrode 9a located in the upper part is promoted to some extent. Furthermore, since the hollow and irregularity which are formed in the front face of pixel electrode 9a in 2nd contact hole 8b are also small and end, flattening in the part of this pixel electrode 9a is promoted to some extent.
[0094] 1st barrier layer 80a consists of a conductive light-shielding film especially with this operation gestalt. Therefore, 1st barrier layer 80a enables it to specify each pixel opening field selectively at least. For example, 1st barrier layer 80a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are an opaque refractory metal, an alloy, metal silicide, etc. Thereby, connection electric good can be taken through contact hole 8b between 1st barrier layer 80a and pixel electrode 9a. As for the thickness of 1st barrier layer 80a, it is desirable to consider for example, as 50nm or more 500nm or less extent. or [that the irregularity of the front face of pixel electrode 9a which possibility of running at the time of puncturing of 2nd contact hole 8b in a manufacture process if there is thickness of about 50nm became low, and originated in existence of 1st barrier layer 80a when it was about 500nm does not serve as a between title] -- or it is because flattening is comparatively easily possible.
[0095] With this operation gestalt, furthermore, the left right-hand side of a field which met data-line 6a among the pixel Sekiguchi fields in each pixel It has specified from the data-line 6a part in island-shape 2nd barrier layer 80b and the contact hole 5 circumference which are extended in the shape of straight side along with data-line 6a. 1st barrier layer 80a and 1st light-shielding film 11a have prescribed the top chord and the lower side of a field which met scanning-line 3a and capacity line 3b among the pixel opening fields in each pixel, respectively.
[0096] As more specifically shown in drawing 2 and drawing 4 , 2nd barrier layer 80b is seen superficially, is selectively arranged in the gap of pixel electrode 9a, and, also selectively, has lapped with pixel electrode 9a. For this reason, by piling up a part of this pixel electrode 9a and 2nd barrier layer 80b can prescribe the great portion of left right-hand side of the pixel opening field in each pixel. Under the present circumstances, especially in the part where the pixel opening field was specified by 2nd barrier layer 80b, since it sees superficially and there is no clearance between pixel electrode 9a and 2nd barrier layer 80b, the optical leakage through such a clearance does not take place. Consequently, eventually, a contrast ratio is raised. Since data-line 6a does not need to prescribe a pixel opening field simultaneously in the part where the pixel opening field was specified by 2nd barrier layer 80b, in this part, the width of face of data-line 6a has been narrowed a little rather than the width of face of 2nd barrier layer 80b. Consequently, as shown in drawing 4 , when making it data-line 6a and pixel electrode 9a not lap through the 3rd interlayer insulation film 7, it is not necessary to generate the parasitic capacitance between the sources of TFT30 and the drains in each pixel. For this reason, it originates in the potential shake concerned of data-line 6a which sways frequently to the potential of the picture signal supplied in predetermined periods, such as one etc. frame, TFT30 of an other bank, TFT30 carries out abnormality actuation with the parasitic capacitance between the above-mentioned source and a drain, and the situation which the electrical potential difference which should be made to hold to pixel electrode 9a leaks can be prevented. The flicker and line nonuniformity in a display image can be reduced these results. however -- the comparatively small field of the contact hole 5 circumference where 2nd barrier layer 80b does not exist -- the width of face of data-line 6a -- some -- thicker ** -- it may be made like and data-line 6a may prescribe a pixel opening field.
[0097] Moreover, if it constitutes so that a pixel opening field may be specified as mentioned above, since it is not necessary to form the 2nd light-shielding film 23 in the opposite substrate 20, it is possible to reduce the cost of an opposite substrate. Furthermore, the lowering and dispersion of a pixel numerical aperture by the alignment gap with the opposite substrate 20 and the TFT array substrate 10 can be prevented. Moreover, when forming the 2nd light-shielding film 23 in the opposite substrate 20 Even if it forms more smallish so that a pixel numerical aperture may not be reduced by the alignment gap with the TFT array substrate 10, as mentioned above Data-line 6a, In order for the film of the protection-from-light nature formed in 1st barrier layer 80a and a 2nd barrier layer 80b list at the TFT array substrate [1st light-shielding film 11a] 10 side to prescribe the pixel Sekiguchi section, Pixel opening can be specified with a sufficient precision and a pixel numerical aperture can be raised compared with the case where pixel opening is decided from 2nd light-shielding film 23 ** on the opposite substrate 20.

[0098] Furthermore, by considering as the configuration which narrows the width of face of data-line 6a a little, and does not lap with a part for the edge of pixel electrode 9a as shown in drawing 2 and drawing 4 Generating of defects, such as an electric short circuit between both with high possibility of generating in the part with which data-line 6a and pixel electrode 9a lapped through the 3rd interlayer insulation film 7 (short circuit), can be suppressed, and decline in the rate of an equipment defect and the improvement in the yield at the time of manufacture are eventually slippery.
[0099] 2nd barrier layer 80b is preferably connected to capacity line 3b or other constant potential lines electrically. That is, since the amount of [of a part for a edge and pixel electrode 9a of 2nd barrier layer 80b] edge laps, some parasitic capacitance is added among both, but if the potential of 2nd barrier layer 80b is maintained at fixed potential, the adverse effect which potential fluctuation of 2nd barrier layer 80b has on the potential of pixel electrode 9a can be reduced. In addition, with this operation gestalt, contact hole 8c for connecting electrically 2nd barrier layer 80b and capacity line 3b can be punctured according to the same process as the process which punctures contact hole 8a, and does not cause complication of a manufacture process. In addition, 2nd barrier layer 80b is electrically connected to capacity line 3b through contact hole 8c in this case for every pixel.
[0100] Furthermore, in the configuration by which opposite arrangement of 2nd barrier layer 80b and the data-line 6a was carried out through the 2nd interlayer insulation film 4 again like ****, capacity is added to data-line 6a between 2nd barrier layer 80b by which potential was stabilized more. For this reason, the capacity of data-line 6a can be set as moderate magnitude which does not cause a potential shake. Even if it makes especially a pixel pitch detailed and makes detailed width of face of data-line 6a in connection with this, the lack of capacity of data-line 6a can be suppressed by making the capacity between 2nd barrier layer 80b increase. Thereby, the write-in deficiency in performance in supply to pixel electrode 9a of the picture signal through data-line 6a can be prevented. In other words, the structure where data-line 6a advantageous in case especially a pixel pitch is made detailed becomes strong to a noise is acquired comparatively easily.
[0101] In addition, although the other shape of a round shape, a square, or a polygon etc. has as the flat-surface configuration of each contact hole (8a, 8b, 8c, and 5) of this operation gestalt, especially a round shape is useful to the crack prevention in the interlayer insulation film around a contact hole etc. And in order to obtain connection electric good, it is desirable to perform wet etching after dry etching and to attach some taper to these contact holes, respectively.
[0102] As explained above, while giving the function to relay TFT30 and pixel electrode 9a to 1st barrier layer 80a according to the electro-optic device of the 1st operation gestalt Since the function to specify a pixel opening field is given closing adequate supply of a picture signal to it if to 2nd barrier layer 80b which consists of the same film as this 1st barrier layer 80a, low cost-ization can be attained in the simplification list of a laminated structure and a manufacture process as a whole.
[0103] (Manufacture process of the electro-optic device in the 1st operation gestalt) Next, the manufacture process of the TFT array substrate which constitutes the electro-optic device in an operation gestalt with the above configurations is explained with reference to drawing 8 from drawing 5 . In addition, it is process drawing which drawing 8 makes each class by the side of the TFT array substrate in each process correspond to the A-A' cross section of drawing 2 like drawing 3 from drawing 5 , and is shown.
[0104] As first shown in the process (1) of drawing 5 , the TFT array substrates 10, such as a quartz substrate, a hard glass substrate, and a silicon substrate, are prepared. Here, it heat-treats preferably at inert gas ambient atmospheres, such as N2 (nitrogen), and an about 900-1300-degree C elevated temperature, and it pretreats so that distortion produced in the TFT array substrate 10 in the elevated-temperature process carried out behind may decrease. That is, according to the temperature by which high temperature processing is carried out at the maximum elevated temperature in a manufacture process, the TFT array substrate 10 is heat-treated at the same temperature or the temperature beyond it in advance. and the whole surface of the TFT array substrate 10 processed in this way -- metal alloy film, such as metal metallurgy group silicide, such as Ti, Cr, W, Ta, Mo, and Pb, -- sputtering etc. -- about 100-500nm thickness -- the light-shielding film 11 of about 200nm thickness is formed preferably. In addition, on a light-shielding film 11, in order to ease a surface echo, antireflection films, such as polish recon film, may be formed.
[0105] Next, as shown in a process (2), 1st light-shielding film 11a is formed by forming the resist mask corresponding to the pattern of 1st light-shielding film 11a by the photolithography on the this formed light-shielding film 11, and etching to a light-shielding film 11 through this resist mask.

[0106] As shown in a process (3), with ordinary pressure or a reduced pressure CVD method on 1st light-shielding film 11a Next, TEOS (tetrapod ethyl orthochromatic silicate) gas, TEB (tetrapod ethyl boat rate) gas, TMOP (tetrapod methyl oxy-FUOSU rate) gas, etc. are used. The substrate insulator layer 12 which consists of silicate glass film, such as NSG (non silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (PORON phosphorus silicate glass), a silicon nitride film, an oxidation silicone film, etc. is formed. The thickness of this substrate insulator layer 12 may be about 500-2000nm.
[0107] Next, as shown in a process (4), about 450-550 degrees C of amorphous silicon film are preferably formed comparatively on the substrate insulator layer 12 with the reduced pressure CVD (for example, CVD with a pressure of about 20-40Pa) using the mono-silane gas of flow rate about 400 to 600 cc/min, disilane gas, etc. of about 500 degrees C in a low-temperature environment. Then, in nitrogen-gas-atmosphere mind, by performing heat treatment of 4 - 6 hours preferably at about 600-700 degrees C for about 1 to 10 hours, solid phase growth of the polish recon film 1 is carried out until it becomes the thickness of about 100nm preferably in about 50-200nm thickness. As an approach of carrying out solid phase growth, heat treatment using RTA (Rapid Thermal Anneal) is sufficient, and laser heat treatment using an excimer laser etc. is sufficient.
[0108] Under the present circumstances, as TFT30 for pixel switching shown in drawing 3 , when creating TFT30 for pixel switching of an n channel mold, the impurity of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn), may be slightly doped by an ion implantation etc. to the channel field concerned. Moreover, when using TFT30 for pixel switching as a p channel mold, the impurity of III group elements, such as B (boron), Ga (gallium), and In (indium), may be slightly doped by an ion implantation etc. In addition, the polish recon film 1 may be directly formed with a reduced pressure CVD method etc. without passing through the amorphous silicon film. Or drive silicon ion into the polish recon film deposited with the reduced pressure CVD method etc., once make it amorphous, it is made to recrystallize by the postheat treatment etc., and the polish recon film 1 may be formed.
[0109] Next, as shown in a process (5), semi-conductor layer 1a which has a predetermined pattern containing the 1f of the 1st storage capacitance electrodes according to a photolithography process, an etching process, etc. is formed.
[0110] As shown in a process (6), semi-conductor layer 1a which constitutes TFT30 for pixel switching next, the temperature of about 900-1300 degrees C, and by oxidizing thermally with the temperature of about 1000 degrees C preferably As thermal oxidation silicone film 2a with a comparatively thin thickness of about 30nm is formed and it is further shown in a process (7) Insulator layer 2b which consists of a high-temperature-oxidation silicone film (HTO film) or a silicon nitride film with a reduced pressure CVD method etc. is deposited on the comparatively thin thickness of about 50nm. The insulating thin film 2 which contains the 1st dielectric film for storage capacitance formation with the gate dielectric film with the multilayer structure containing thermal oxidation silicone film 2a and insulator layer 2b of TFT30 for pixel switching is formed. consequently, the thickness of semi-conductor layer 1a -- the thickness of about 30-150nm -- desirable -- the thickness of about 35-50nm -- becoming -- the thickness of the insulating thin film 2 -- the thickness of about 20-150nm -- it becomes the thickness of about 30-100nm preferably. Thus, by shortening elevated-temperature thermal oxidation time amount, when using especially an about 8 inches large-sized substrate, the camber by heat can be prevented. However, the insulating thin film 2 with monolayer structure may be formed only by oxidizing the polish recon film 1 thermally.
[0111] Next, as shown in a process (8), after forming the resist layer 500 according to a photolithography process, an etching process, etc. on semi-conductor layer 1a except the part used as the 1f of the 1st storage capacitance electrodes, P ion is doped in about 3x1012/cm2 of doses, and the 1f of the 1st storage capacitance electrodes is formed into low resistance.
[0112] Next, as shown in a process (9), after removing the resist layer 500, the polish recon film 3 is deposited with a reduced pressure CVD method etc., thermal diffusion of the P is carried out further, and the polish recon film 3 is electric-conduction-ized. or low [into which the polish recon film 3 formed simultaneously introduced P ion] -- the polish recon film [****] may be used. The thickness of the polish recon film 3 is preferably deposited on about 300nm in about 100-500nm thickness.
[0113] Next, as shown in the process (10) of drawing 6 , capacity line 3b is formed with scanning-line 3a of a predetermined pattern according to a photolithography process, an etching process, etc. using a resist mask. Scanning-line 3a and capacity line 3b are good also as a multilayer interconnection which could form by metal alloy film, such as refractory metal metallurgy group silicide, and was combined

with the polish recon film etc.
[0114] Next, as shown in a process (11), when TFT30 for pixel switching shown in drawing 3 is set to TFT of an n channel mold with LDD structure, In order to form low concentration source field 1b and low concentration drain field 1c in semi-conductor layer 1a first, by using as a mask the gate electrode which consists of a part of scanning-line 3a, it is low concentration about the impurity of V group elements, such as P, for example, P ion is doped with the dose of one to 3x1013-/cm2. Thereby, semi-conductor layer 1a under scanning-line 3a becomes channel field 1a'. Capacity line 3b and scanning-line 3a are also formed into low resistance by the dope of this impurity.
[0115] Next, as show in a process (12), in order to form 1d of high concentration source fields and high concentration drain field 1e which constitute TFT30 for pixel switching, after form the resist layer 600 on scanning line 3a with a mask with wide width of face rather than scanning line 3a, similarly it be high concentration about the impurity of V group elements, such as P, for example, P ion be dope with the dose of 1 - 3x1015-/cm2. Moreover, to semi-conductor layer 1a, when using TFT30 for pixel switching as a p channel mold, in order to form 1d of high concentration source fields, and high concentration drain field 1e in low concentration source field 1b and a low concentration drain field 1c list, the impurity of III group elements, such as B, is used and doped. In addition, it is good also as TFT of offset structure, without, for example, performing a low-concentration dope, and it is good also as TFT of a self aryne mold by the ion-implantation technique using P ion, B ion, etc., using scanning-line 3a as a mask. Capacity line 3b and scanning-line 3a are also further formed into low resistance by the dope of this impurity.
[0116] In addition, in parallel to these component formation processes of TFT30, circumference circuits with the **** type structure which consists of an n channel mold TFT and a p channel mold TFT, such as a data-line actuation circuit and a scanning-line actuation circuit, may be formed in the periphery on the TFT array substrate 10. Thus, if semi-conductor layer 1a which constitutes TFT30 for pixel switching in this operation gestalt is formed by the polish recon film, at the time of formation of TFT30 for pixel switching, it is the same process mostly, and a circumference circuit can be formed and it is advantageous on manufacture.
[0117] Next, as shown in a process (13), after removing the resist layer 600, the 1st interlayer insulation film 81 which consists of a high-temperature-oxidation silicone film (HTO film) or a silicon nitride film by the reduced pressure CVD method, a plasma-CVD method, etc. is deposited [capacity line 3b and a scanning-line 3a list] on the insulating thin film 2 at the comparatively thin thickness of about 200nm or less. However, as mentioned above, the 1st interlayer insulation film 81 may be constituted from a multilayer, and can form the 1st interlayer insulation film 81 with various kinds of well-known techniques used for generally forming the gate dielectric film of TFT.
[0118] Next, as shown in a process (14), contact hole 8c for connecting electrically 2nd barrier layer 80b and capacity line 3b to the contact hole 8a list for connecting electrically 1st barrier layer 80a and high concentration drain field 1e is formed by dry etching, such as reactive ion etching and reactant ion beam etching. Since such dry etching has high directivity, it can puncture contact hole 8a and contact hole 8c of a small path. Or wet etching advantageous to preventing that contact hole 8a runs through semi-conductor layer 1a may be used together. This wet etching is effective also from a viewpoint which gives the taper for taking connection more electric to fitness to contact hole 8a. Moreover, especially contact hole 8a and contact hole 8c can be simultaneously punctured to **** like, and are advantageous to it on manufacture.
[0119] Next, as shown in a process (15), all over capacity line 3b looked into through high concentration drain field 1e and contact hole 8c which are looked into through contact hole 8a in 1st interlayer insulation film 81 list, metal alloy film, such as metal metallurgy group silicide, such as Ti, Cr, W, Ta, Mo, and Pb, is deposited by sputtering etc., and the electric conduction film 80 of about 50-500nm thickness is formed. If there is thickness of about 50nm, there will almost be no possibility of running when puncturing contact hole 8b behind. In addition, on this electric conduction film 80, in order to ease a surface echo, antireflection films, such as polish recon film, may be formed. In addition, the electric conduction film 80 may be a multilayer which carried out the laminating of the metal alloy film or polish recon film, such as metal metallurgy group silicide.
[0120] Next, as shown in the process (16) of drawing 7 , 1st barrier layer 80a and 2nd barrier layer 80b are formed by performing a photolithography process, an etching process, etc. on the this formed electric conduction film 80. As especially 2nd barrier layer 80b was shown in drawing 4 here, it is good to form so that it may lap pixel electrode 9a in which the part is formed later, and a little.

[0121] Next, as shown in a process (17), the 2nd interlayer insulation film 4 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, an oxidation silicone film, etc. is formed using ordinary pressure or a reduced pressure CVD method, TEOS gas, etc. so that 1st barrier layer 80a and 2nd barrier layer 80b may be covered in 1st interlayer insulation film 81 list. The thickness of the 2nd interlayer insulation film 4 has desirable about 500-1500nm. If there is 500nm or more of thickness of the 2nd interlayer insulation film 4, the parasitic capacitance between data-line 6a and scanning-line 3a will remain, or will hardly pose a problem.
[0122] Next, in order to activate semi-conductor layer 1a, after heat-treating about 10000-degreeC about 20 minutes in the phase of a process (18), the contact hole 5 for connecting electrically high concentration drain field 1e of data-line 6a and semi-conductor layer 1a is punctured to the insulating thin film 2, the 1st interlayer insulation film 81, and the 2nd interlayer insulation film 4. Moreover, the contact hole for connecting with wiring which illustrates neither scanning-line 3a nor capacity line 3b in a substrate boundary region can also be punctured according to the same process as a contact hole 5.
[0123] Next, as shown in a process (19), it deposits preferably in about 100-500nm thickness by sputtering etc. on the 2nd interlayer insulation film 4 at about 300nm by making low resistance metal metallurgy group silicide, such as aluminum of protection-from-light nature, etc. into a metal membrane 6.
[0124] Next, as shown in a process (20), data-line 6a is formed according to a photolithography process, an etching process, etc. As especially data-line 6a was shown in drawing 4 here, it forms so that it may not lap with pixel electrode 9a formed later, and so that it may lap with 2nd barrier layer 80b.
[0125] Next, as shown in the process (21) of drawing 8 , the 3rd interlayer insulation film 7 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, an oxidation silicone film, etc. is formed using ordinary pressure or a reduced pressure CVD method, TEOS gas, etc. so that a data-line 6a top may be covered. The thickness of the 3rd interlayer insulation film 7 has desirable about 500-1500nm.
[0126] Next, as shown in a process (22), contact hole 8b for connecting electrically pixel electrode 9a and 1st barrier layer 80a is formed by dry etching, such as reactive ion etching and reactant ion beam etching. Wet etching may be added in order to make it the shape of a taper.
[0127] Next, on the 3rd interlayer insulation film 7, as shown in a process (23), as the transparent conductive thin films 9, such as ITO film, are deposited on the thickness of about 50-200nm and are further shown in a process (24) by sputtering etc., pixel electrode 9a is formed according to a photolithography process, an etching process, etc. In addition, when using the electro-optic device concerned as a reflective mold, pixel electrode 9a may be formed from an opaque ingredient with high reflection factors, such as aluminum.
[0128] As explained above, according to the manufacture process in this operation gestalt, the electro-optic device of the 1st operation gestalt which is a comparatively small routing counter and was mentioned above using each comparatively easy process can be manufactured.
[0129] (The 2nd operation gestalt) The configuration of the electro-optic device in the 2nd operation gestalt of this invention is explained with reference to drawing 11 from drawing 9 . Drawing 9 is a top view of two or more pixel groups where the TFT array substrate with which the data line in the 2nd operation gestalt, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 10 is the A-A' sectional view, and drawing 11 is the B-B' sectional view. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for each class or every each part material in drawing 10 and drawing 11 . In addition, about the same component as the 1st operation gestalt shown in drawing 4 from drawing 2 in the 2nd operation gestalt shown in drawing 11 from drawing 9 , the same reference mark is attached and the explanation is omitted.
[0130] It has junction conductive layer 6b which is electrically connected to high concentration drain field 1e of semi-conductor layer 1a through contact hole 88a with the 2nd operation gestalt in drawing 11 from drawing 9 , and consisted of same layers as data-line 6a, and 1st barrier layer 90a which consists of a conductive layer of the protection-from-light nature electrically connected to pixel electrode 9a through contact hole 88c. And opposite arrangement is carried out through the 2nd interlayer insulation film 4 formed on data-line 6a and junction conductive layer 6b, and junction conductive layer 6b and 1st barrier layer 90a are mutually connected electrically through contact hole 88b punctured by this 2nd interlayer insulation film 4. On the other hand, with the 2nd operation gestalt, 2nd barrier layer 90b which consists of a conductive layer of the same protection-from-light nature as 1st barrier layer 90a is

prepared, and 2nd barrier layer 90b and capacity line 3b are electrically connected through contact hole 88d. It can substitute as a capacity line by using 2nd barrier layer 90b as a storage capacitance electrode, and connecting it with an adjoining pixel group by this. In this case, you may form in island shape for every pixel by using capacity line 3b as a storage capacitance electrode. Thereby, a pixel numerical aperture can be enlarged. Moreover, by connecting electrically 2nd barrier layer 90b and capacity line 3b, it can be double, a capacity line can be formed and redundant structure can be realized. As shown in drawing 9 , except for the perimeter of the field where it sees superficially and 1st barrier layer 90a exists, the gap of pixel electrode 9a is established in 2nd barrier layer 90b in the shape of a wrap grid, and it specifies the left right-hand side which met data-line 6a and scanning-line 3a among pixel opening fields, respectively, and the vertical side. Also in this case, a part for the edge of 2nd barrier layer 90b is put on a part for the edge of pixel electrode 9a a little as well as the case of the 1st operation gestalt. In addition, about the gap of 1st barrier layer 90a and 2nd barrier layer 90b, optical leakage can be easily prevented by covering by the 2nd light-shielding film 23 by the side of junction conductive layer 6b or an opposite substrate. About other configurations, it is the same as that of the case of the 1st operation gestalt.

[0131] Thus, with the 2nd operation gestalt, junction becomes possible good about from pixel electrode 9a to semi-conductor layer 1a by junction conductive layer 6b and 1st barrier layer 90a which are two conductive layers for junction. When pixel electrode 9a consists of ITO film and data-line 6a consists of aluminum film especially, it is desirable to constitute from refractory metals, such as Ti, Cr, W, etc. from which connection electric good is obtained among both, etc.

[0132] Moreover, as shown in drawing 11 , in the configuration by which data-line 6a was pinched through the 1st interlayer insulation film 81 and the 2nd interlayer insulation film 4 which are a dielectric film between capacity line 3b and barrier layer 90b, capacity is added to data-line 6a between capacity line 3b and 2nd barrier layer 90b by which potential was stabilized more. For this reason, the capacity of data-line 6a can be set as moderate magnitude which does not cause a potential shake, and the write-in deficiency in performance in supply to pixel electrode 9a of the picture signal through data-line 6a can be prevented.

[0133] Junction conductive layer 6b which consists of the same film as such aluminum film For example, it sets at the process (18) in the manufacture process of the 1st operation gestalt. Puncture contact hole 88a which results in high concentration drain field 1e, and in a process (20), although junction conductive layer 6b is formed above high concentration drain field 1e including the part of this contact hole 88a What is necessary is just to give a photolithography process, an etching process, etc. to aluminum film formed at the process (19). What is necessary is just to form according to the same process as a process (16) from the process (13) in the 1st operation gestalt furthermore at 2nd interlayer insulation film 4 list on data-line 6a and junction conductive layer 6b about 1st barrier layer 90a and 2nd barrier layer 90b.

[0134] (The 3rd operation gestalt) The configuration of the electro-optic device in the 3rd operation gestalt of this invention is explained with reference to drawing 12 . Drawing 12 is a sectional view corresponding to the sectional view in which the data line in the 3rd operation gestalt, the scanning line, a pixel electrode, etc. were formed. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for each class or every each part material in drawing 12 . In addition, about the same component as the 2nd operation gestalt shown in drawing 10 in the 3rd operation gestalt shown in drawing 12 , the same reference mark is attached and the explanation is omitted.

[0135] In drawing 12 , without using junction conductive layer 6b unlike the 2nd operation gestalt, it consists of 3rd operation gestalten so that electric connection can be taken between direct high concentration drain field 1e by 1st barrier layer 90a'. About other configurations, it is the same as that of the case of the 2nd operation gestalt.

[0136] Therefore, according to the 3rd operation gestalt, trunk connection of pixel electrode 9a and the high concentration drain field 1e can be electrically carried out by 1st barrier layer 90a' constituted from congenial refractory metal film by the ITO film which constitutes pixel electrode 9a, and the electric target.

[0137] (The 4th operation gestalt) The configuration of the electro-optic device in the 4th operation gestalt of this invention is explained with reference to drawing 15 from drawing 13 . Drawing 13 is a top view of two or more pixel groups where the TFT array substrate with which the data line in the 4th operation gestalt, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 14 is

the A-A' sectional view, and drawing 15 is the B-B' sectional view. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for each class or every each part material in drawing 14 and drawing 15 . In addition, about the same component as the 1st operation gestalt shown in drawing 4 from drawing 2 in the 4th operation gestalt shown in drawing 15 from drawing 13 , the same reference mark is attached and the explanation is omitted.

[0138] In drawing 15 , the gap of pixel electrode 9a where 1st light-shielding film 11a' adjoins each other unlike the 1st operation gestalt is sewn with the 4th operation gestalt from drawing 13 , it is formed in the shape of a grid, and capacity line 3b is electrically connected to 1st protection-from-light gland 11a' for every pixel through the contact hole 15. The potential of storage capacitance 70 can be stabilized by it being possible to operate 1st light-shielding film 11a' as redundancy wiring of capacity line 3b, and attaining low resistance-ization of capacity line 3b. Moreover, this configuration may constitute capacity line 3b from substituting for 1st light-shielding film 11a' as a capacity line as an island-shape storage capacitance electrode for every pixel. Thereby, a pixel numerical aperture can be enlarged. Moreover, the capacity line for forming storage capacitance may be made 3-fold wiring by combining with the 2nd operation gestalt by connecting capacity line 3b with 1st light-shielding film 11a' and 2nd barrier layer 90b electrically. When forming in island shape for every pixel by using capacity line 3b as a storage capacitance electrode, 1st light-shielding film 11a' and 2nd barrier layer 90b are connected with the pixel which is electrically connected through a storage capacitance electrode, and adjoins. In addition, the faulty connection in a contact hole 15 and contact hole 8c can be prevented by puncturing in the flat-surface location where contact hole 8c for connecting a contact hole 15, 2nd barrier layer 80b, and capacity line 3b differs.

[0139] Furthermore, as shown in drawing 14 and drawing 15 , wiring and a part of TFTat least 30 become depressed in a concave, TFT array substrate 10' is formed, and the upside front face is formed evenly. Consequently, flattening of the front face of the 3rd interlayer insulation film 7 in the plane region in which wiring of data-line 6a, scanning-line 3a, capacity line 3b, etc. and TFT30 were formed is carried out. About other configurations, it is the same as that of the case of the 1st operation gestalt.

[0140] Therefore, according to the 4th operation gestalt, a level difference with a pixel opening field with the field where scanning-line 3a, TFT30, capacity line 3b, etc. are formed in the data line 6 in piles is reduced. Thus, since flattening of the pixel electrode 9a is carried out, the disclination of the liquid crystal layer 50 can be reduced according to the degree of the flattening concerned. Consequently, more nearly high-definition image display becomes possible and it also becomes possible to extend a pixel opening field.

[0141] In addition, it may carry out by for example, not flattening by forming a slot in such TFT array substrate 10' but CMP (Chemical Mechanincal Polishing) processing, spin coat processing, the reflow method, etc., or flattening in the 2nd interlayer insulation film 4 or the 3rd interlayer insulation film 7 may be performed using the organic SOG (Spin On Glass) film, the inorganic SOG film, the polyimide film, etc. In addition, an above-mentioned configuration is applicable also to the 1st operation gestalt, the 2nd operation gestalt, and the 3rd operation gestalt.

[0142] (The whole electro-optic device configuration) The whole electro-optic device configuration in each operation gestalt constituted as mentioned above is explained with reference to drawing 16 and drawing 17 . In addition, drawing 16 is the top view which looked at the TFT array substrate 10 from the opposite substrate 20 side with each component formed on it, and drawing 17 is the H-H' sectional view of drawing 16 .

[0143] In drawing 16 , on the TFT array substrate 10, the sealant 52 is formed along the edge and the 3rd light-shielding film 53 as a frame which specifies the circumference of the image display field which consists of an ingredient which is the same as the 2nd light-shielding film 23, or is different is formed in parallel to the inside. The data-line actuation circuit 101 and the external circuit connection terminal 102 which drive data-line 6a by supplying a picture signal to data-line 6a to predetermined timing are prepared in the field of the outside of a sealant 52 along with one side of the TFT array substrate 10, and the scanning-line actuation circuit 104 which drives scanning-line 3a is formed along with two sides which adjoin this one side by supplying a scan signal to scanning-line 3a to predetermined timing. If the scan signal delay supplied to scanning-line 3a does not become a problem, the thing only with one side sufficient [the scanning-line actuation circuit 104] cannot be overemphasized. Moreover, the data-line actuation circuit 101 may be arranged on both sides along the side of an image display field. For example, the data line of an odd number train supplies a picture signal from the data-line actuation

circuit arranged along one side of an image display field, and you may make it the data line of an even number train supply a picture signal from the data-line actuation circuit arranged along the side of the opposite hand of said image display field. Thus, if it is made to drive the data line in the shape of a ctenidium, since the occupancy area of a data-line actuation circuit is extensible, it becomes possible to constitute a complicated circuit. Furthermore, two or more wiring 105 for connecting between the scanning-line actuation circuits 104 established in the both sides of an image display field is formed in one side in which the TFT array substrate 10 remains. Moreover, in at least one place of the corner section of the opposite substrate 20, the flow material 106 for taking an electric flow between the TFT array substrate 10 and the opposite substrate 20 is formed. And as shown in drawing 17 , the opposite substrate 20 with the almost same profile as the sealant 52 shown in drawing 16 has fixed to the TFT array substrate 10 by the sealant 52 concerned. In addition, on the TFT array substrate 10, the inspection circuit for inspecting the sampling circuit which impresses a picture signal to two or more data-line 6a to predetermined timing, the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it to two or more data-line 6a respectively, the quality of the electro-optic device concerned at the manufacture middle or the time of shipment, a defect, etc. in addition to these data-line actuation circuits 101 and scanning-line actuation circuit 104 grade etc. may be formed. In addition, according to the gestalt of this operation, the 2nd light-shielding film 23 on the opposite substrate 20 can be easily removed by the application of an electro-optic device that what is necessary is just to form smaller than the protection-from-light field on the TFT array substrate 10.

[0144] You may make it connect with LSI for actuation mounted on the TAB (Tape Automated bonding) substrate instead of forming the data-line actuation circuit 101 and the scanning-line actuation circuit 104 on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10 with each operation gestalt explained with reference to drawing 17 from drawing 1 above. Moreover, according to the exception of modes of operation, such as TN (Twisted Nematic) mode, VA (Vertically Aligned) mode, and PDLC (Polymer Dispersed Crystal) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, the polarization version, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.

[0145] Since the electro-optic device in each operation gestalt explained above is applied to a projector, the electro-optic device of three sheets will be respectively used as a light valve for RGB, and incidence of the light of each color respectively decomposed through the dichroic mirror for RGB color separation will be respectively carried out to each light valve as incident light. Therefore, with each operation gestalt, the light filter is not prepared in the opposite substrate 20. However, the light filter of RGB may be formed in the predetermined field which counters pixel electrode 9a in which the 2nd light-shielding film 23 is not formed on the opposite substrate 20 with the protective coat. If it does in this way, the electro-optic device in each operation gestalt is applicable to the color electro-optic device of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 20. Or it is also possible to form a light filter layer in the bottom of pixel electrode 9a which counters RGB on the TFT array substrate 10 by a color resist etc. If it does in this way, a bright electro-optic device is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 20 again may be formed. According to this opposite substrate with a die clo ITSUKU filter, a brighter color electro-optic device is realizable.

[0146] Although [the electro-optic device in each operation gestalt explained above] incidence of the incident light is carried out from the opposite substrate 20 side as usual, since 1st light-shielding film 11a (or 11a') is prepared, incidence of the incident light is carried out from the TFT array substrate 10 side, and it may be made to carry out outgoing radiation from the opposite machine hill 20 side. That is, even if it attaches an electro-optic device in a projector in this way, it can prevent light carrying out incidence to channel field 1a' of semi-conductor layer 1a, low concentration source field 1b, and low concentration drain field 1c, and it is possible to display a high-definition image. Although the polarizing plate with which AR (Anti Reflection) coat was carried out for acid resisting needs to be arranged separately or AR film needed to be stuck here in order to prevent the echo by the side of the

rear face of the TFT array substrate 10 conventionally With each operation gestalt, since [of the front face of the TFT array substrate 10, and semi-conductor layer 1a] 1st light-shielding film 11a (or 11a') is formed at least between channel field 1a', low concentration source field 1b, and low concentration drain field 1c, Such a polarizing plate and AR film by which AR coat was carried out are used, or the need of using the substrate which carried out AR processing of TFT array substrate 10 itself is lost. Therefore, according to each operation gestalt, ingredient cost can be reduced, and a contaminant, a blemish, etc. do not drop the yield at the time of polarizing plate attachment, and it is very advantageous. Moreover, since lightfastness is excellent, even if it uses the bright light source, or it carries out polarization conversion by the polarization beam splitter and it raises efficiency for light utilization, image quality degradation of the cross talk by light etc. is not produced.

[0147] Moreover, although explained as a switching element prepared in each pixel that it was the poly-Si TFT of a forward stagger mold or a coplanar mold, each operation gestalt is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0148] (Electronic equipment) Next, the gestalt of operation of electronic equipment equipped with the electro-optic device 100 explained to the detail above is explained with reference to drawing 20 from drawing 18 .

[0149] The outline configuration of the electronic equipment which equipped drawing 18 with the electro-optic device 100 in this way is shown first.

[0150] In drawing 18 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the actuation circuit 1004, an electro-optic device 100, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a picture signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the actuation circuit 1004 with a clock signal CLX. The actuation circuit 1004 drives an electro-optic device 100. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes an electro-optic device 100, the actuation circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.

[0151] Next, the example of the electronic equipment constituted in this way from drawing 19 by drawing 20 is shown respectively.

[0152] In drawing 19 , an example slack projector 1100 of electronic equipment prepares three light valves with which the actuation circuit 1004 mentioned above contains the electro-optic device 100 carried on the TFT array substrate, and is constituted as a projector respectively used as light valves 100R, 100G, and 100B for RGB. In a projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be respectively led to the light valves 100R, 100G, and 100B corresponding to each color. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors respectively modulated with light valves 100R, 100G, and 100B is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.

[0153] In drawing 20 , the electro-optic device 100 mentioned above is formed in the top covering case, and other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while they hold CPU, memory, a modem, etc. further.

[0154] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal,

and touch panel other than electronic equipment which were explained with reference to drawing 20 from drawing 19 above etc. is mentioned as an example of the electronic equipment shown in drawing 18 .

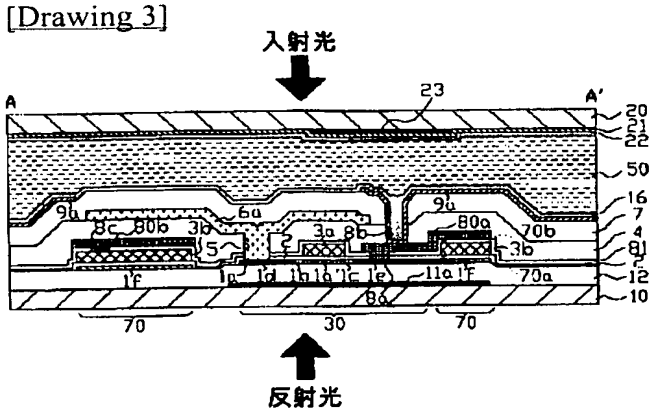
[0155] As explained above, according to the gestalt of this operation, various kinds of electronic equipment equipped with the electro-optic device in which high-definition image display with high manufacture effectiveness is possible is realizable.

[Translation done.]

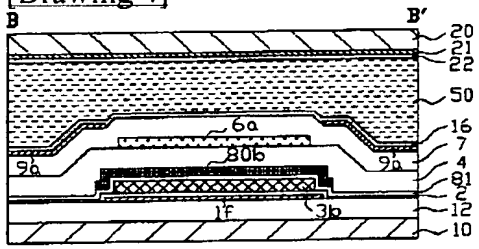
* NOTICES *

DRAWINGS

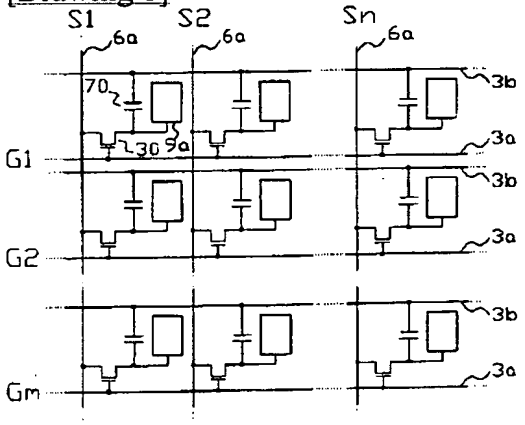
[Drawing 3]



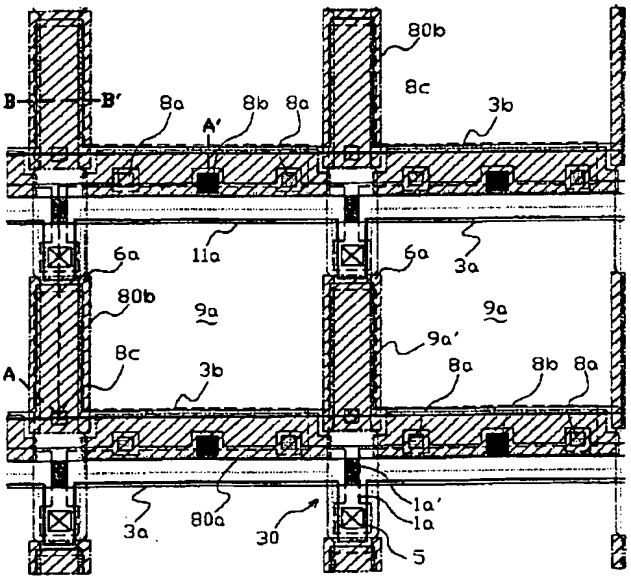
[Drawing 4]



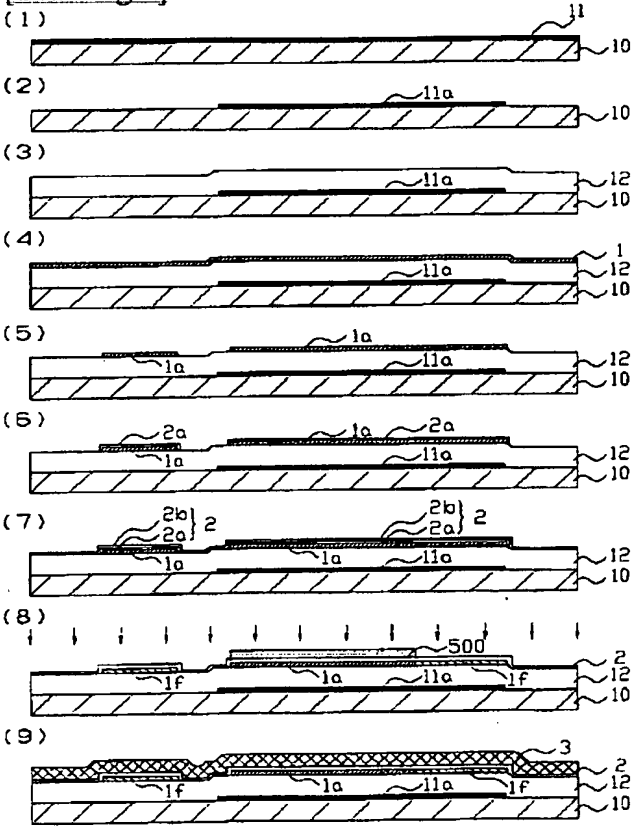
[Drawing 1]



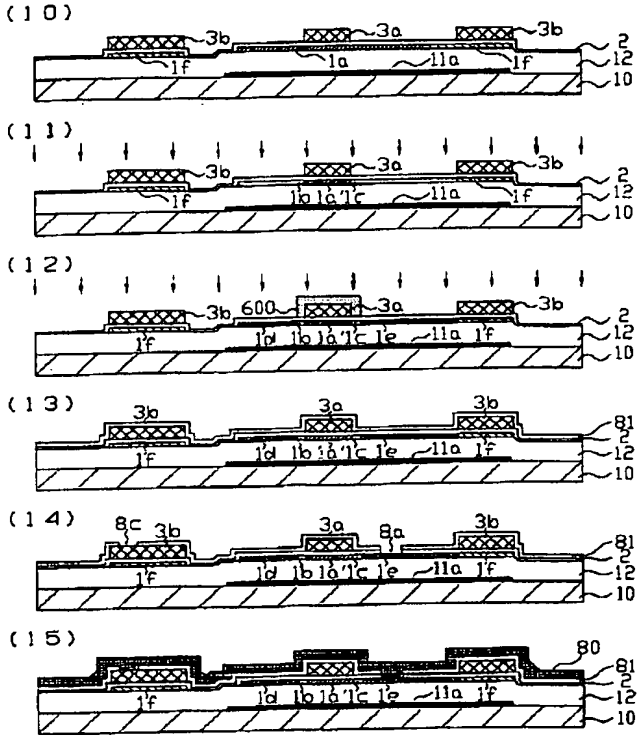
[Drawing 2]



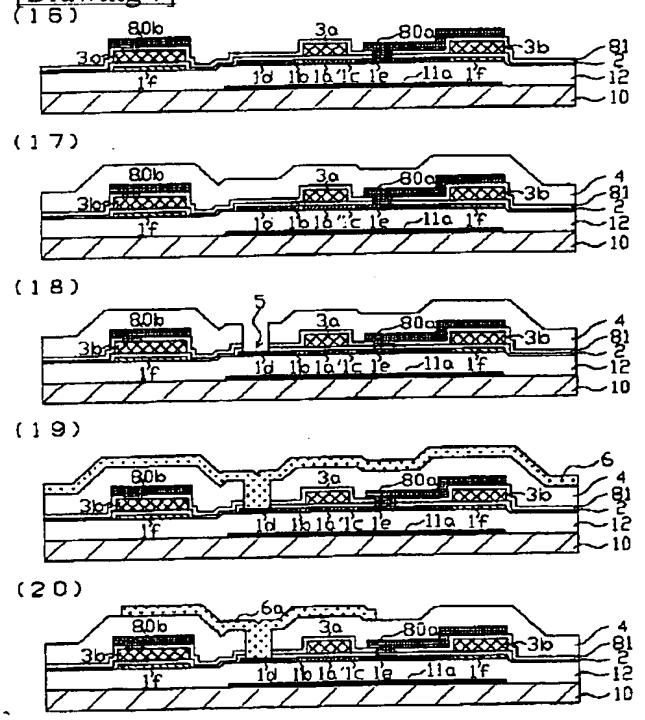
[Drawing 5]



[Drawing 6]

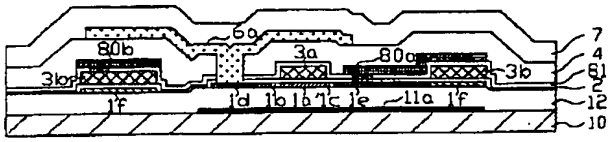


[Drawing 7]



[Drawing 8]

(21)



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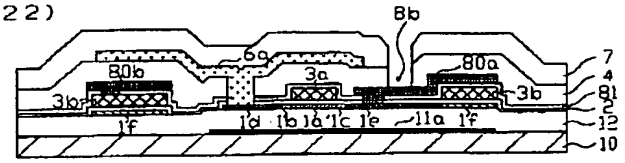

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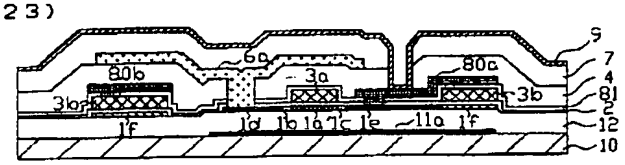

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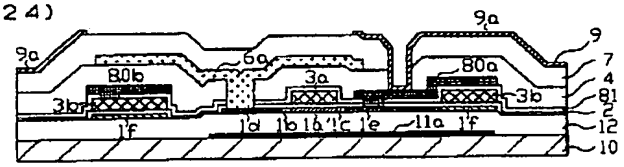
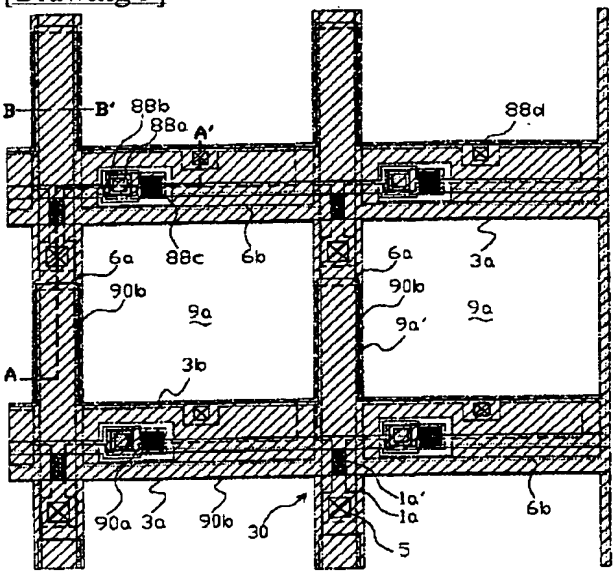
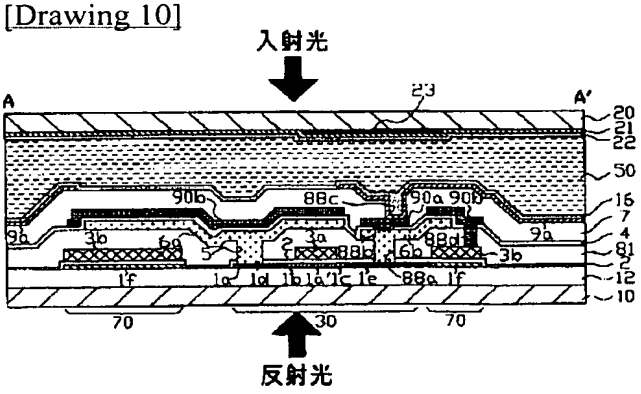


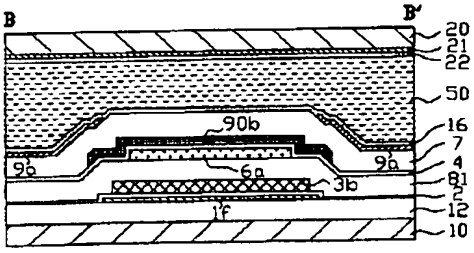
[Drawing 9]



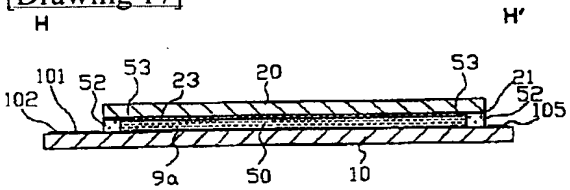
[Drawing 10]



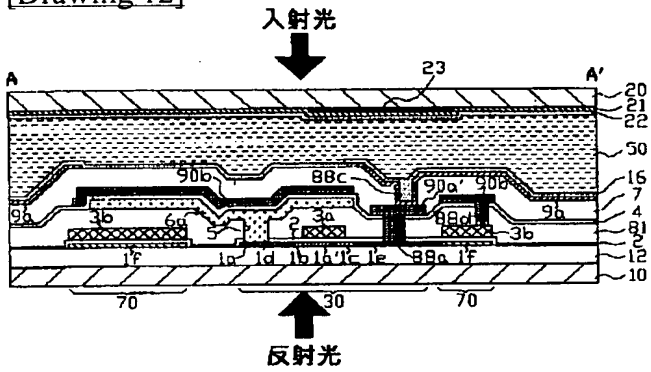
[Drawing 11]



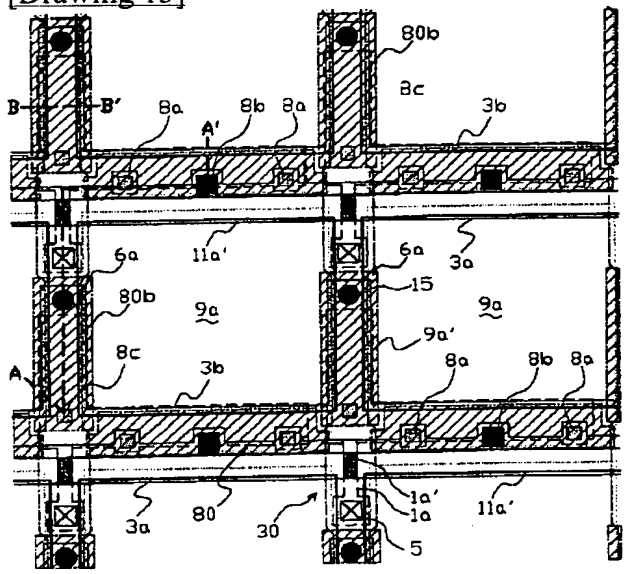
[Drawing 17]



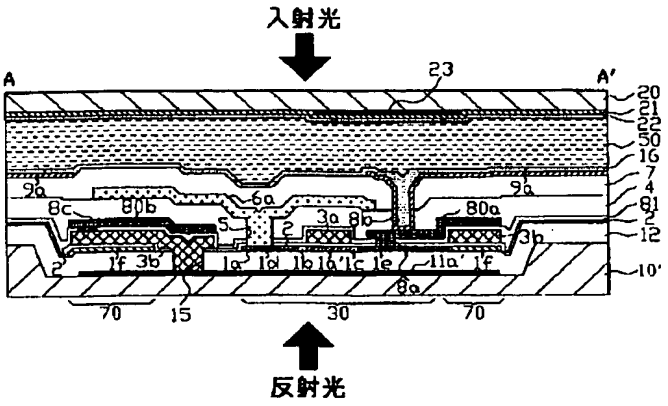
[Drawing 12]



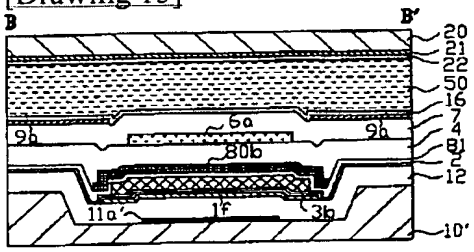
[Drawing 13]



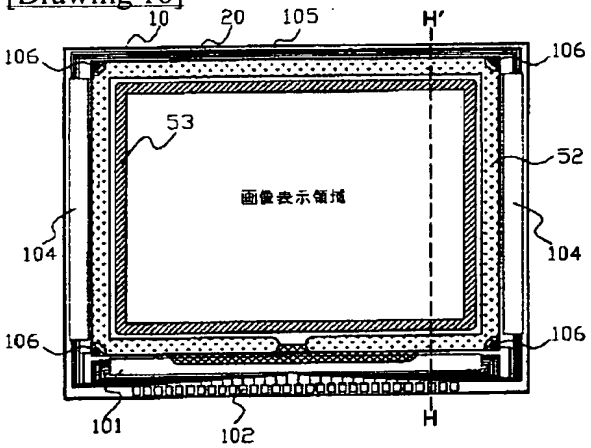
[Drawing 14]



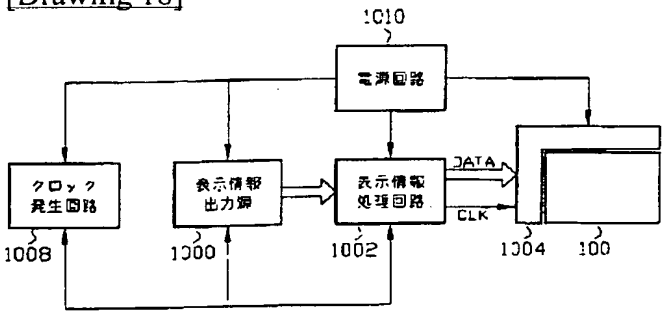
[Drawing 15]



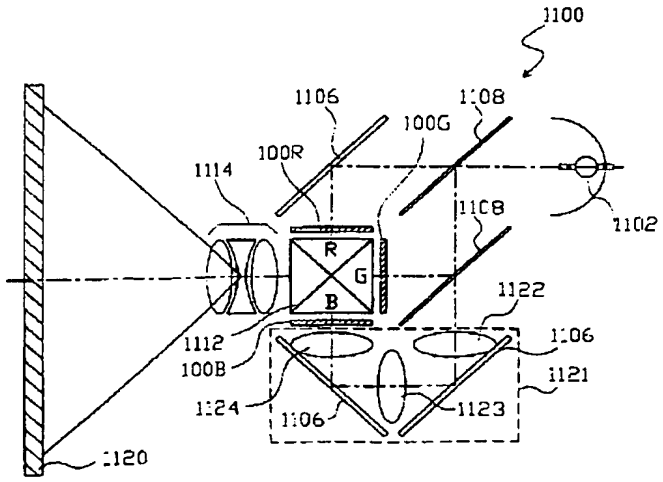
[Drawing 16]



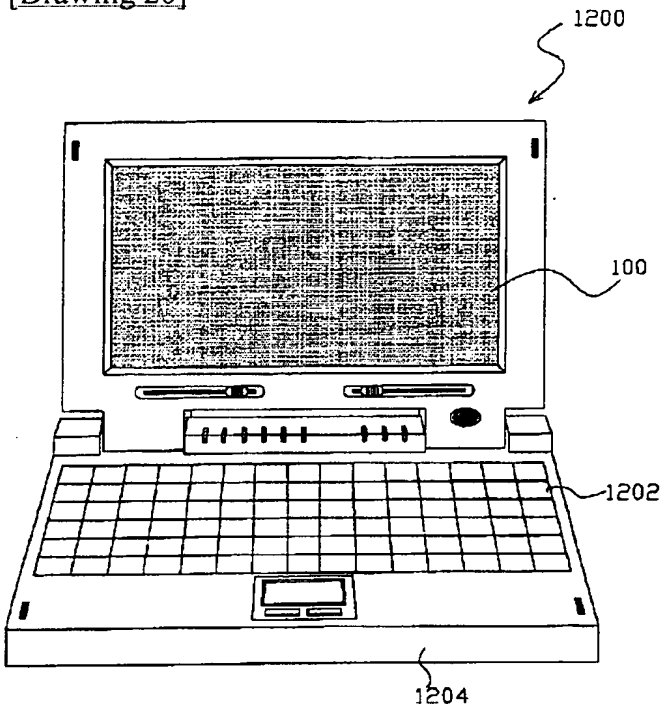
[Drawing 18]



[Drawing 19]



[Drawing 20]



[Translation done.]

* NOTICES *

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Category partition] The 2nd partition of the 6th category
[Publication date] September 24, Heisei 16 (2004. 9.24)

[Publication No.] JP,2001-249625,A (P2001-249625A)
[Date of Publication] September 14, Heisei 13 (2001. 9.14)
[Application number] Application for patent 2000-271562 (P2000-271562)
[The 7th edition of International Patent Classification]

G09F 9/30
G02F 1/1335
G02F 1/1368
H01L 29/786

[FI]

G09F 9/30 330 Z
G02F 1/1335 500
G02F 1/136 500
H01L 29/78 612 C
H01L 29/78 619 B

[Procedure amendment]
[Filing Date] September 11, Heisei 15 (2003. 9.11)
[Procedure amendment 1]
[Document to be Amended] Description
[Item(s) to be Amended] The name of invention
[Method of Amendment] Modification
[The content of amendment]
[Title of the Invention] An electro-optic device and electronic equipment
[Procedure amendment 2]
[Document to be Amended] Description
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[The content of amendment]
[Claim(s)]
[Claim 1]
It is the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, and a pixel electrode,
The 1st junction conductive layer which was electrically connected to the semi-conductor layer of said thin film transistor, and was formed by the same film as said data line,
The light-shielding film which is formed in the upper layer and specifies a pixel opening field selectively at least from said data line,
The field where said light-shielding film was removed selectively,

The 2nd junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed selectively, and was connected to said 1st junction conductive layer and electric target,
The electro-optic device characterized by providing the pixel electrode electrically connected to said 2nd junction conductive layer.
[Claim 2]
It is the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, and a pixel electrode,
The light-shielding film which is formed in the upper layer and specifies a pixel opening field selectively at least from said data line,
The field where said light-shielding film was removed selectively,
The junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed selectively, and was connected to the semi-conductor layer and the electric target of said thin film transistor,
The electro-optic device characterized by providing the pixel electrode electrically connected to said junction conductive layer.
[Claim 3]
The field where said light-shielding film was removed selectively is an electro-optic device according to claim 1 or 2 characterized by being formed in the field of the light-shielding film between said adjoining data lines.
[Claim 4]
An electro-optic device given in any 1 term of claim 1 characterized by having the 1st storage capacitance electrode formed in the drain field of said semi-conductor layer, and the 2nd storage capacitance electrode which is formed by the same film as the gate electrode of said thin film transistor, and laps with said 1st storage capacitance electrode thru/or claim 3.
[Claim 5]
Said drain field is an electro-optic device according to claim 4 characterized by being formed along with said scanning line.
[Claim 6]
Said drain field is an electro-optic device according to claim 4 or 5 characterized by being formed along with said data line.
[Claim 7]
Said light-shielding film is an electro-optic device given in any 1 term of claim 4 which is constant potential and is characterized by connecting said 2nd storage capacitance electrode with said light-shielding film electrically thru/or claim 6.
[Claim 8]
The electrical installation of said light-shielding film and said 2nd storage capacitance electrode is an electro-optic device according to claim 7 characterized by being formed in the field of the light-shielding film between said adjoining data lines.
[Claim 9]
Electronic equipment characterized by having the electro-optic device of a publication in any 1 term of claim 1 to claim 8.
[Procedure amendment 3]
[Document to be Amended] Description
[Item(s) to be Amended] 0009
[Method of Amendment] Modification
[The content of amendment]
[0009]
[Means for Solving the Problem]
In order that the electro-optic device of this invention may solve the above-mentioned technical problem, this invention is characterized by the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line and a pixel electrode possessing the following. The 1st junction conductive layer which was electrically connected to the semi-conductor layer of said thin film transistor, and was formed by the same film as said data line The light-shielding

film which is formed in the upper layer and specifies a pixel opening field selectively at least from said data line The field where said light-shielding film was removed selectively The pixel electrode electrically connected to the 2nd junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed selectively, and was connected to said 1st junction conductive layer and electric target, and said 2nd junction conductive layer

Moreover, this invention is characterized by the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line and a pixel electrode possessing the following, in order that the electro-optic device of this invention may solve the above-mentioned technical problem. The light-shielding film which is formed in the upper layer and specifies a pixel opening field selectively at least from said data line The field where said light-shielding film was removed selectively The junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed selectively, and was connected to the semi-conductor layer and the electric target of said thin film transistor The pixel electrode electrically connected to said junction conductive layer

Moreover, it is characterized by equipping this invention with the following. To a substrate, they are two or more scanning lines. Two or more data lines The thin film transistor and pixel electrode which have been arranged corresponding to the crossover of said each scanning line and each of said data line The 1st conductive layer of the protection-from-light nature which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, and was connected to said semi-conductor layer and electric target, and was connected to said pixel electrode and electric target, and the 2nd conductive layer which consisted of the same film as said 1st conductive layer, saw superficially, and has lapped with said data line selectively at least

[Procedure amendment 4]

[Document to be Amended] Description

[Item(s) to be Amended] 0062

[Method of Amendment] Modification

[The content of amendment]

[0062]

The scanning line of plurality [approach / of the electro-optic device of this invention / manufacture / substrate], and two or more data lines, In the manufacture approach of an electro-optic device of having the thin film transistor connected to said each scanning line and said each data line, and the pixel electrode to which said thin film transistor was connected The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance in the predetermined field on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures ** 1 contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, So that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 2nd insulator layer The 1st conductive layer of protection-from-light nature, The process which forms the 2nd conductive layer from the same film as said 1st conductive layer, and the process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd **********, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It has the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer is formed so that it may see superficially and may lap with said data line selectively at least.

[Procedure amendment 5]

[Document to be Amended] Description

[Item(s) to be Amended] 0063

[Method of Amendment] Modification

[The content of amendment]

[0063]

According to the manufacture approach of the electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the 1st contact hole which leads to a semi-conductor layer is punctured by an insulating thin film and the 1st interlayer insulation film, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a semi-conductor layer electrically through this 1st contact hole. The 2nd conductive layer is formed so that it may be selectively arranged at least in the gap of the field in which it sees superficially and a pixel electrode is simultaneously formed from the same film as this 1st conductive layer. Then, laminating formation of the 2nd interlayer insulation film, the data line, and the 3rd interlayer insulation film is carried out in this order. Next, the 2nd contact hole which leads to the 1st conductive layer is punctured, and pixel ionization formation is carried out so that it may connect with the 1st conductive layer electrically through this 2nd contact hole. Therefore, the electro-optic device of this invention which has the configuration which forms the 1st and 2nd conductive layers as a layer near a substrate, and relays a pixel electrode and a semi-conductor layer by the 2nd conductive layer through two contact holes rather than the data line mentioned above can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[Procedure amendment 6]
[Document to be Amended] Description
[Item(s) to be Amended] 0064
[Method of Amendment] Modification
[The content of amendment]
[0064]
In the mode of 1 of the manufacture approach of said electro-optic device of this invention In the process which forms said data line after the process which forms said 2nd interlayer insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.

[Procedure amendment 7]
[Document to be Amended] Description
[Item(s) to be Amended] 0066
[Method of Amendment] Modification
[The content of amendment]
[0066]
This invention is characterized by the manufacture approach of an electro-optic device that the manufacture approach of other electro-optic devices of this invention has the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate possessing the following. The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate The process which forms an insulating thin film on said semi-conductor layer The process which forms one electrode of the scanning line and storage capacitance on said insulating thin film The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it

may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer

[Procedure amendment 8]
[Document to be Amended] Description
[Item(s) to be Amended] 0067
[Method of Amendment] Modification
[The content of amendment]
[0067]
According to the manufacture approach of the electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the contact hole which leads to a semi-conductor layer is punctured, and a junction conductive layer is formed from the same film as the data line so that it may connect with a semi-conductor layer electrically, at the same time the data line is formed. Next, after the 2nd interlayer insulation film is formed, the contact hole which leads to a junction conductive layer is punctured, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a junction conductive layer electrically. It can come, simultaneously the 2nd conductive layer is formed from the same film as the 1st conductive layer. Then, the 3rd interlayer insulation film is formed, the contact hole which leads to the 1st conductive layer is punctured, and a pixel electrode is formed so that it may connect with the 1st conductive layer electrically. Therefore, as the layer further than the data line from a substrate, i.e., the upper layer, while forming a junction conductive layer as a conductive layer which consists of the same film as the data line mentioned above, the 1st conductive layer is formed, and while relaying a pixel electrode and a semi-conductor layer by the junction conductive layer and the 1st conductive layer through three contact holes, the electro-optic device of this invention which has the configuration which specifies a pixel opening field by the 2nd conductive layer can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[Procedure amendment 9]
[Document to be Amended] Description
[Item(s) to be Amended] 0068
[Method of Amendment] Modification
[The content of amendment]
[0068]
In the mode of 1 of the manufacture approach of said electro-optic device of this invention In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film and said 2nd interlayer insulation film at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[Translation done.]